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The Discussion and strategy of PDN impedance design

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Abstract

All industries have one common feature: Easy to get started but difficult to master. After learning the POWERRAC simulation method for netizens studying the method described in the "Signal and Power Integrity Simulation Design and High-Speed Product Application Examples" book, they can solve the common problems in the project PowerAC problems, but with the deepening of learning and research, many new problems have been encountered and more needs have been put forward, such as: When will the project PI simulation intervene;How to achieve accurate and rapid evaluation of capacitor modeling; How to optimize the capacitance on the existing PCB according to cost, quantity, type, area, etc. How to reduce the comprehensive cost of the existing PCB . In response to the above problems, this article will conduct a detailed discussion, and finally give the corresponding process and strategy.

Keywords

PDN ;Decoupling capacitor;Target impedance.

1. PCB decoupling capacitor recommendations

In the component Datasheet about how to decouple, the decoupling recommendation will most often be described as follows: "The supply to this pin should be decoupled with 0.1uF and 0.01uF Capacitor to ground as near as possible", as shown in the following figure, These suggestions are summed up in 2 points:

"Use 0.1uF or 0.01uF capacitor"

"The closer to power management, the better"

Pin No.	Pin Name	Description
J15	OOBPLL_VAALV	Analog Power Supply for the Out-of-Band Demodulator (ADC). Nominal Voltage at this pin is 1.2V ± 0.06V (preliminary voltage value, subject to change) • The supply to this pin should be decoupled with 1.0µF and 0.1µF capacitors to ground as near the device as possible. • The proximity of the 0.1µF capacitor to the device should be prioritized. • Contact Entropic Application Engineers regarding analog supply filtering requirements for specific applications.
H7	VDDAPLL_LV	Analog Power Supply for PLL. Nominal Voltage at this pin is 1.2V ± 0.06V (preliminary voltage value, subject to change) • The supply to this pin should be decoupled with 0.1µF and 0.01µF capacitors to ground as near the device as possible. • The proximity of the 0.01µF capacitor to the device should be prioritized. • Contact Entropic Application Engineers regarding analog supply filtering requirements for specific applications.

Fig. 1 Application suggestions for filter capacitors on a Datasheet

This kind of advice seems to be omnipotent, but it will be a "headache" when it is applied in engineering days: many times it is impossible to achieve it due to the actual application environment, not to mention the application of each board is very different!

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In response to the recommendations on the Datasheet, hardware engineers generally strictly implement or over-design, and often give the downstream schematic diagram as follows:

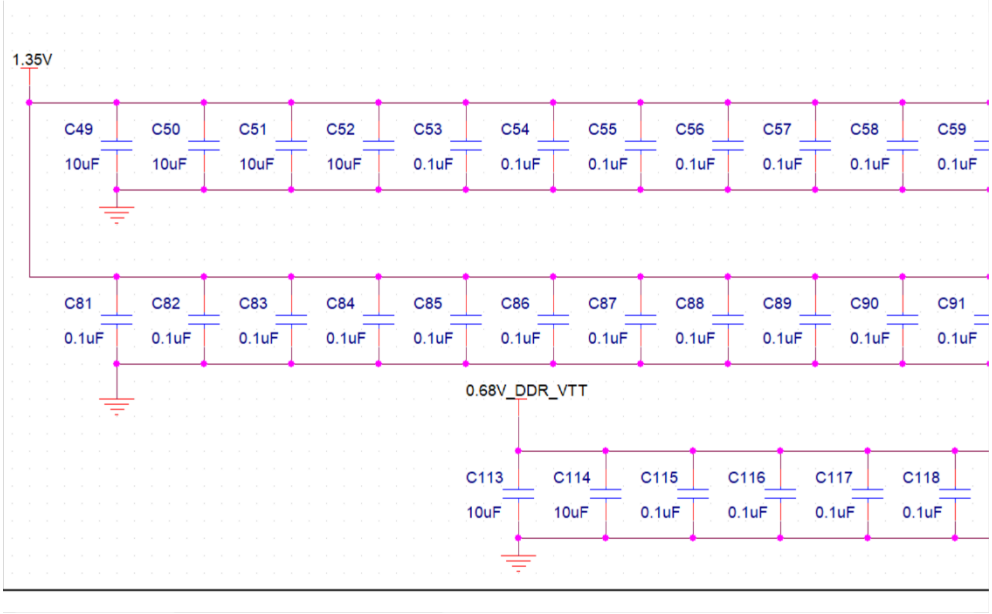

Fig. 2 The schematic diagram of common capacitor combinations

Try to copy as much as possible in the schematic diagram, and find that there is no space to put more capacitors in the PCB design, and finally delete it. This method has no quantitative details on the PCB design from the aspects of the number, position, and type combination of capacitors. The reason became the one mentioned at the beginning: the more the better, the closer the better.

In fact, these problems can be intervened at different stages through the correct process, design, and simulation methods, and an ideal solution that is more realistic can be obtained.

2. Initial assessment and strategy

How to effectively determine the project's capacitor filtering scheme is the most critical step in the early stage of the project. The industry's mature EDA tools can provide a more elaborate capacitor design in the early stage of the project: including the combination of capacitance value, placement, and whether the target impedance is satisfied Such as processing according to the corresponding process can reduce the overall cost and reduce rework.

Target impedance

The specific steps of the initial capacitance evaluation and formulation strategy are as follows: the first choice is to determine the target resistance, and the early PI is to determine the target impedance using the following method.

$$Z_{\text{Target}} = \frac{\text{Power supply vol tage} \times \text{Allowed Ripple}}{\text{Current}}$$

This estimation method will consider the influence of various parasitic inductances when the current is increasing, and the target impedance using a minimum line can no longer adapt

Start using the frequency-dependent target impedance curve as shown below, which makes it easier to meet the target impedance value during simulation.

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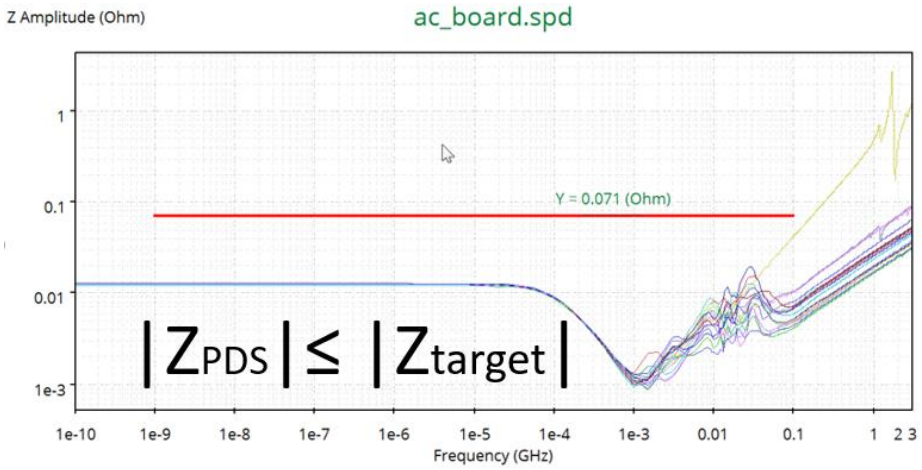

Fig.3 Rough assessment of early target impedance

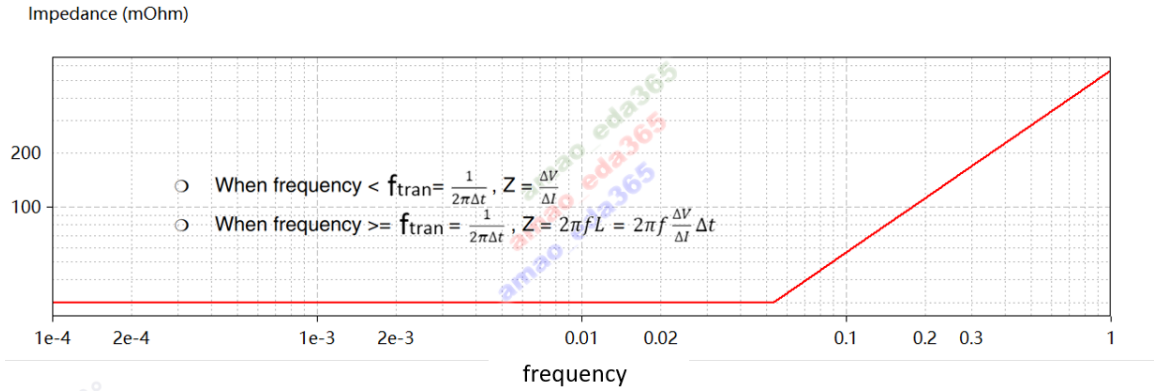

Fig. 4 Target blocking optimization

But for low voltage and large current, the current target impedance evaluation is still too rough. It requires a detailed flip of the logic gate and buffer and a precise capacitance in a cycle to get the target impedance that meets the requirements, which is often very difficult. Therefore, the focus will shift to the design and strategy of capacitor decoupling in the package and inside the chip.

Capacitor combination and fine design

In the early stage of the layout, you can confirm: the position range of the capacitor, the number of capacitors, the combination of the capacitance value, and the Fanout form used. These steps are completed in the initial stage, and the completion of the later layout can basically meet the target impedance requirements, even The adjustment is only a small local adjustment.

3. Middle and late period of the project

The SI engineer will perform a PowrAC simulation on the board after the board is completed to see if the impedance curve meets the target impedance requirements in many cases:

The impedance curve has a higher resonance at some frequencies, but it does not exceed the target impedance.

The target impedance is only a few MHz.

For the first case, general engineers are reluctant to deal with it. For the second case, they will try to improve by adding higher frequency capacitors. If you don't have a good method and apply the corresponding software work, it will be a more cumbersome manual. Iterative work, so choosing software that includes various optimization items (including smallest cost, smallest capacitor type, smallest capacitor type etc.) is a very wise choice for PI simulation optimization.

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Excellent software will give you multiple strategies The results are available for selection, as shown in the results below.

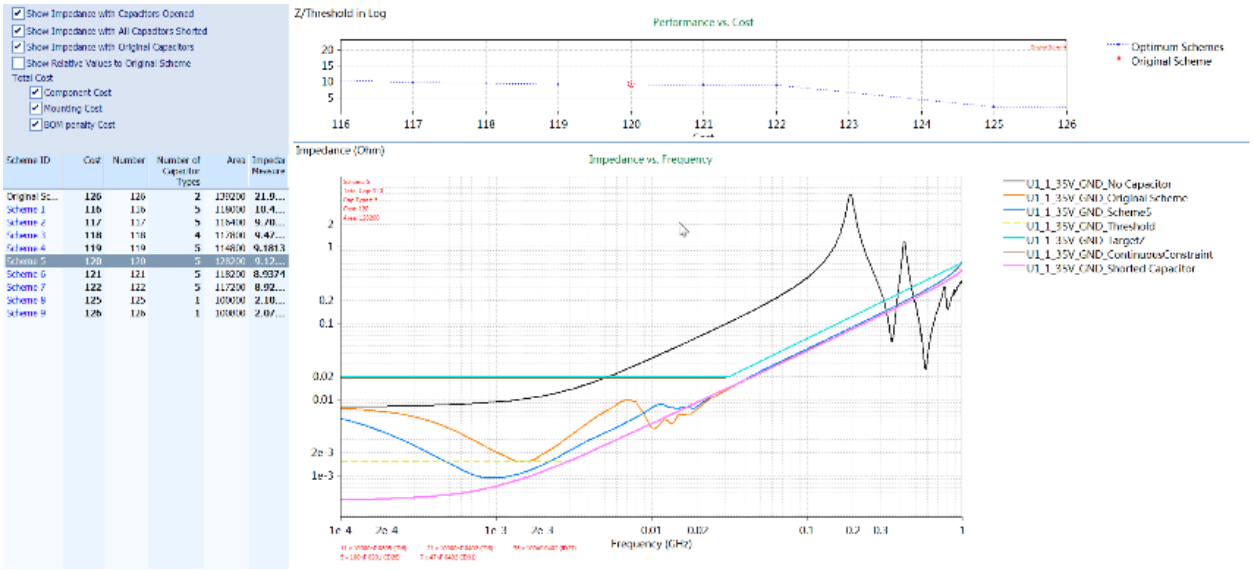

Fig. 5 Simulation effect completed in the early stage

Another way is not to change the current capacitance position and size, but to change the optimization requirements of the capacitance value combination. As shown in the figure below, this way can quickly get results by using the method similar to What if.

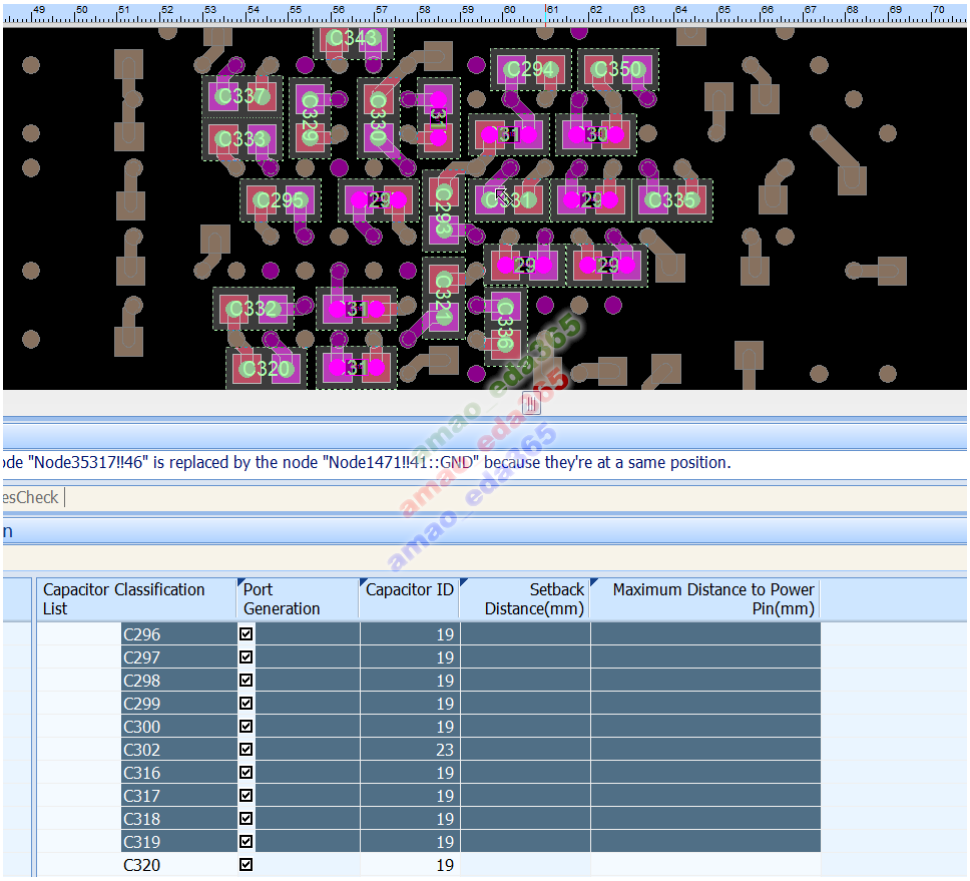

Fig. 6 What if Class Optimization for selected capacitors

However, if the target impedance is set too strictly artificially, the optimization result will not be obtained, or the optimization result will not be achieved at all. Therefore, a good design is not obtained through the optimization in the later stage, but basically finalized at the early stage of the project, and only needs minor adjustment in the later stage.

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4. Capacitance model and management

In the simulation process of the project, different software processes different models of capacitance. It is very important to provide a set of accurate models to ensure the accuracy of the results. The capacitance model can be provided by the supplier or measured by itself. Due to the influence of each parasitic parameter, the simulation results of the capacitance of different models will be different, as shown in the figure below, the same capacitance, when using S parameter and RLC model, the simulation results will find some deviation.

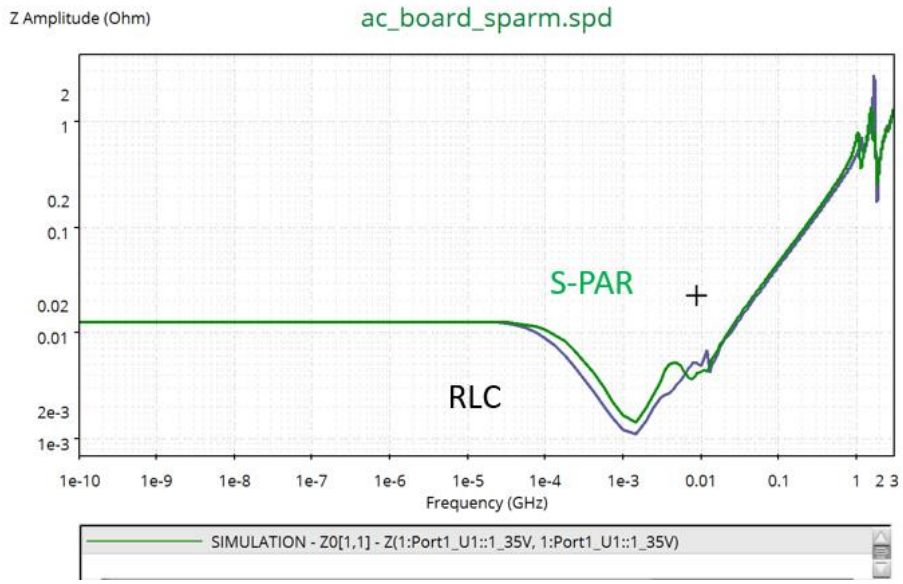

Fig. 7 Comparison of simulation results using S parameter and RLC

5. Conclusion

To sum up, in powerac simulation, we should intervene in the early stage of the project and give a detailed and feasible scheme, so that the workload of PDN optimization in the later stage will be very small, and preparing a set of accurate capacitance model library can better ensure the accuracy of simulation.

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