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Low-Power, High-Transient Response Capacitors-Less Low-Dropout Regulator

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Abstract

This thesis designs a Low-Dropout Regulator (LDO) circuit with low power consumption and high transient response. This design is mainly used to supply power to the digital part of the digital-analog chip. A two-stage operational amplifier is used as the error amplifier of the LDO, and the frequency compensation method adopts nested miller compensation (NMC), and a slew rate enhancement circuit is added to improve its transient response under low power consumption. This design adopts 0.35μmCMOS process, the simulation results show that the quiescent current of this LDO is only 7.9μA, and the linear regulation rate and load regulation rate are 0.047mV/V and 0.043mV/A, respectively. The load range is 100μA-50mA, the load capacitance is 0pF-100pF, the heavy load to light load settling time is 0.3μs, and the light load to heavy load settling time is 2.7μs.

Keywords

Capacitors-Less low-dropout regulator; low power; high transient response; slew rate enhancement.

1. Introduction

As energy saving and environmental protection become hot topics of discussion today, power management chips have become an indispensable class of chips in consumer electronics. Power management chips are mainly divided into the following categories: linear regulators, switching DC-DC converters, charge pumps and PMUs. Among them, the advantages of linear regulators are that there are few peripheral devices and low noise, but they can only be stepped down, and the conversion efficiency is low. DC-DC can be boosted and stepped down and has high conversion efficiency, but there are many peripheral devices, resulting in electromagnetic interference, large size and high cost. The PMU can switch between multiple modes, but it also has problems such as electromagnetic interference, and the cost is also the highest among these power management chips. In this design, the linear regulator is chosen as the most research object.

In traditional LDO circuits, an off-chip load capacitor is usually added to the output of the chip. On the one hand, the overshoot voltage can be suppressed when the load jumps. On the other hand, a zero point can be introduced inside the unity gain bandwidth through the parasitic equivalent resistance of the off-chip capacitor to offset the influence of the main pole and improve the stability of the LDO feedback loop. sex. However, as the chip integration becomes higher and higher, and in the digital-analog hybrid chip, the external capacitance method not only increases the area of the PCB board, but also increases the pins of the chip, which undoubtedly increases the chip area and cost. Therefore, the research and design of LDOs without off-chip capacitors has become a popular research direction for power management chips.

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The main design difficulties of LDO without off-chip capacitors mainly include the following two points: The first is to suppress the overshoot voltage of the output terminal. Since there is no charge and discharge of the large capacitor at the output end, when the load is switched, the power transistor cannot provide or reduce the output current in time, which may easily lead to overshoot and undershoot at the output end. Undershoot may cause insufficient power supply to the load and cannot work normally, and overshoot may easily cause the load to exceed the rated voltage. By adding a slew rate enhancement circuit [1, 2] to the gate of the output power tube, the turn-on and turn-off speed of the MOS tube can be improved, and the overshoot and undershoot can be reduced. However, some slew rate enhancement circuits are large in scale [3] and are not suitable for low-power application scenarios. So this paper adopts a small slew rate enhancement circuit to improve the transient response of the power tube. The second is the loop stability of LDOs without off-chip capacitors. When there is no off-chip capacitor to cancel the influence of the main pole through the pole, how to improve the loop stability becomes the first problem to be solved. Common compensation schemes include wide-bandwidth error amplifier and zero-pole tracking compensation, and the second is the combination of narrow-bandwidth error amplifier and miller compensation. In addition, the compensation method of adaptive power supply [4] or current mirror compensation [5]. Since this design adopts a two-stage error amplifier structure, this paper adopts the combination of narrow bandwidth error amplifier and miller compensation. For the miller compensation method, this paper adopts the nested miller compensation method with the help of the design method of the three-stage operational amplifier [6].

2. Proposed Circuit

In order to achieve the design purpose of low power consumption, this text adopts the structure of two-stage error amplifier. In order to get better stability and load capacity, the method of narrow bandwidth error amplifier plus nested miller compensation is adopted in this paper. To improve the transient response of the entire LDO, a transient enhancement circuit is added to this design. The specific circuit schematic diagram is as follows:

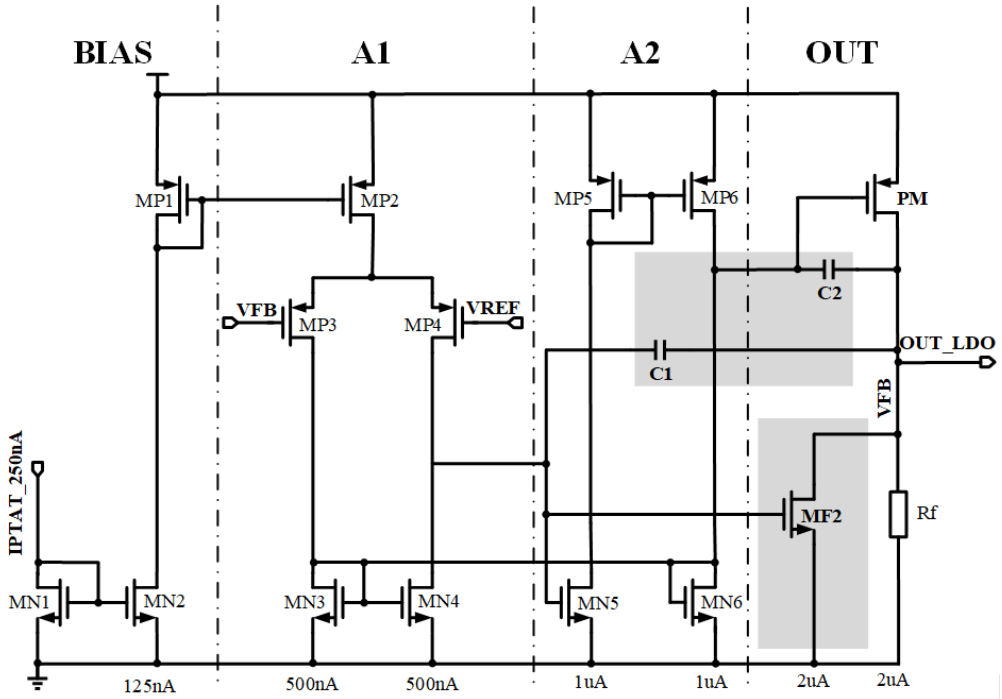

Fig.1 Circuit Schematic of LDO

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As shown in Fig 1, the LDO of this design mainly includes four parts, namely the bias module (BIAS), the first stage error amplifier (A1), the second stage error amplifier (A2) and the output stage (OUT). The input of the bias module is the proportional to absolute temperature (PTAT) current provided by the bandgap reference, which is then converted into a voltage through a current mirror to bias the first-stage operational amplifier. The first-stage operational amplifier adopts a dual-input single-output common-source amplifier, the second-stage operational amplifier also adopts a common-source amplifier, and the output stage adopts a PMOS tube as a power tube.

In order to improve the driving ability of the second-stage error amplifier to the gate of the power tube, the bias current of the second-stage amplifier is increased, and the two branches consume a total of 2uA. Combined with the design index of the maximum load of 20mA, a PMOS tube with a size of 16*200um/300nm is used as its power tube. When the load current is a heavy load of 20mA, the power tube can work normally in the saturation region. When the load is a light load At 100μA, it works in the sub-threshold region, which meets the design requirements. Because the reference voltage and output voltage are both 1.2V and the feedback coefficient is 1, the feedback loop of this LDO only uses a feedback resistor R_f. According to the requirement of the minimum quiescent current of 10μA, a current of 2μA is set to the output stage, so the value of R_f is 600KΩ, the ideal power consumption of the whole LDO is about 8.8μA.

The compensation method used in this design is NMC. It can be seen from the references and analysis that there are three poles in this circuit, as follows:

$$P_1 = -\frac{1}{R_1 C_1 g_{M2} R_2 g_{M3} R_3} \tag{1}$$

$$P_2 = -\frac{1}{R_2 C_2 \left(1 + g_{M3} R_3\right)} \tag{2}$$

$$P_3 = -\frac{1}{R_3 C_L} \tag{3}$$

R_* and g_{M*} are the output resistance and transconductance of the corresponding stage, respectively. It can be seen that in order to realize the stability of the loop, it must be guaranteed that $P_1 \ll GBW \ll P_2 \ll P_3$ in all working modes, and GBW is the bandwidth of the LDO loop.

According to the theoretical analysis of the three-stage op amp in the reference. Since the Butterworth low-pass filter is the flattest in the bandwidth, this response is used as the Butterworth response to guide the zero-pole distribution of the three-stage op amp. According to the references, the modified Butterworth response should satisfy the following conditions:

$$GBW = \frac{1}{4}\left(\frac{g_{M3} - g_{M2}}{C_L}\right) = \frac{g_{M1}}{C_1} = \frac{g_{M3} g_{M2}}{2\left(g_{M3} - g_{M2}\right) C_2} \tag{4}$$

And because of the problem that the zero point of the right half plane is earlier than the zero point of the left plane of the inevitable parameter in the transfer function of the three-stage op amp, which affects its phase margin and stability, so in addition to using the NMC compensation method, this design adds a third feedback loop, The function of g_{MF2} is to cancel the effect of the zero point of the right half plane, improve the phase margin, improve the GBW, and improve the transient response.

To achieve the effect of Butterworth response when g_{MF2} is added, the following design conditions should be satisfied according to reference [6]:

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$$GBW = \frac{1}{4}\left(\frac{g_{M3} + g_{MF2} - g_{M2}}{C_L}\right) = \frac{g_{M1}}{C_1} = \frac{g_{M3}g_{M2}}{2\left(g_{M3} + g_{MF2} - g_{M2}\right)C_2} \quad (5)$$

In addition, g_{MF2} should be larger than g_{M2}, and C_1 and C_2 should be larger than the output capacitance of the corresponding output terminals, respectively. Set the *GBW* of the LDO open loop to 2MHz, and invert the compensation capacitors C_1 and C_2. The relevant parameters are as follows:

Table. 1 Main parameters of the device

g_{M3}@100uA(A/V)	*GBW*(Hz)	g_{M1}(A/V)	Scheme 3	g_{M2}(A/V)	g_{MF2}(A/V)	C_1(F)	C_2(F)
2M	2M	7μ	20μ	40μ	3.5p	5p	200p

The addition of MOS transistor MF2 can also enhance the discharge current capability of the output branch. Since the gate of MF2 is connected to the positive input of the first-stage error amplifier, when switching from heavy load to light load, the output branch has no time to discharge excess At this time, the output terminal of the first stage op amp has the same polarity as the LDO output terminal, and an overshoot signal also appears. Use this signal to increase the on-current of MF2 to help The output branch discharges excess current to improve transient response. The MF2 tube is biased at a small current during normal operation, so as not to increase power consumption, and because gMf2 should be greater than g_{M2}, a 2μA bias current is chosen as a compromise.

3. Simulation Results

This design uses SMIC 0.13μm CMOS process to design and simulate the LDO of this design.

At room temperature and standard process angle, the quiescent current consumed by this LDO is 7.922μA, which meets the specifications of low-power design. When the power supply voltage variation range is between 2.5V-3.6V, observe the LDO output voltage variation range and calculate the linear regulation. The simulation results are shown in Figure 2. The maximum output voltage change is 51.668μV, and the corresponding linear regulation is 0.047mV/V.

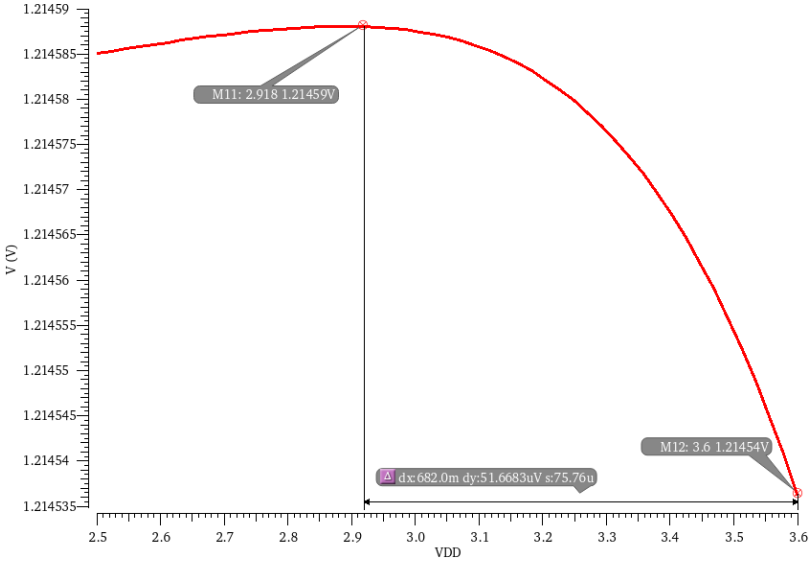

Fig.2 Linear regulation simulation results

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The load current is scanned in the range of 100μA-20mA, and the curve of the output voltage changing with the load current is obtained. As shown in Figure 3, the maximum output voltage change is 858.6nV, and the corresponding load regulation rate is 0.043mV/A.

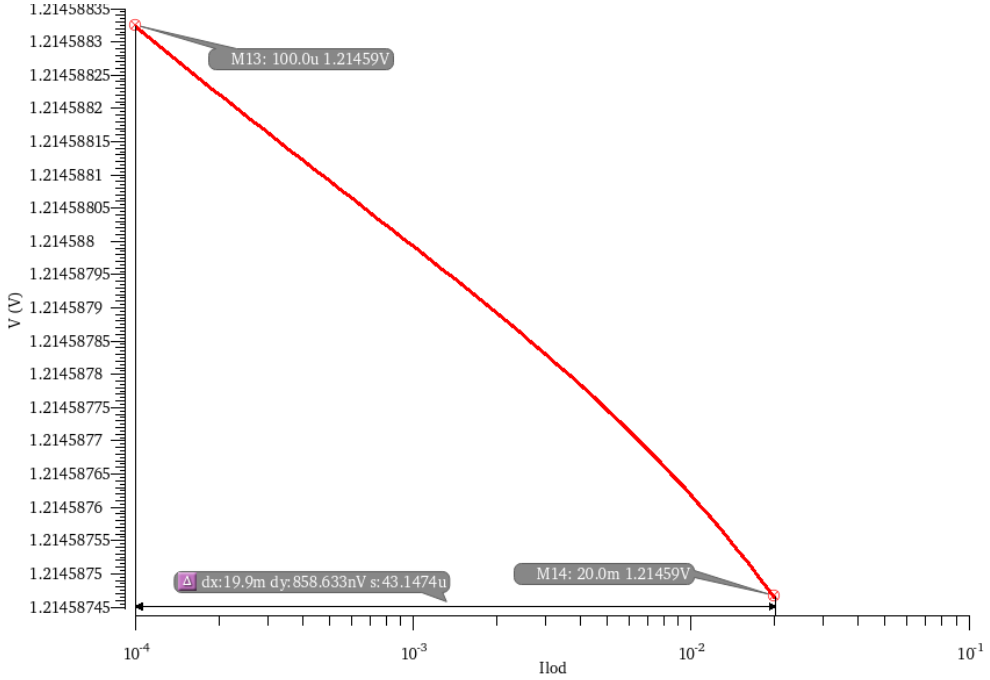

Fig.3 Load regulation simulation results

Figure 4 shows the transient simulation results of the load switching between 20mA and 100μA. It can be seen from the figure that the switching time of the load switching from 20mA to 100μA is 1ns, and the output voltage recovery time is 308.69ns; the recovery time of the load switching from 100μA to 20mA is 2.69μs.

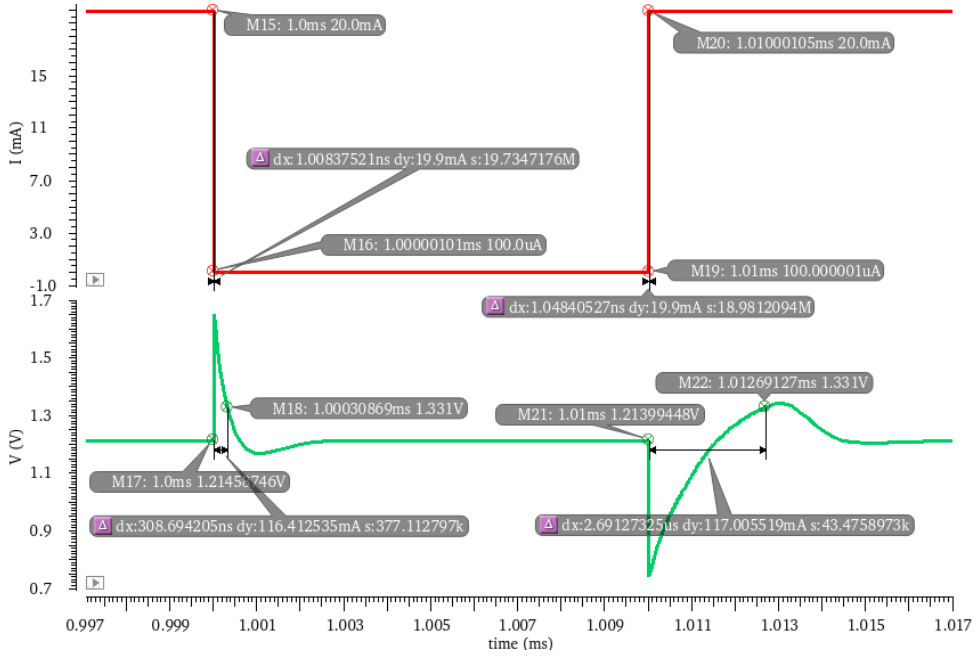

Fig.4 Transient response simulation results

The stability analysis of the entire LDO loop is carried out to obtain the simulation results in Figure 5. It can be seen from the figure that under the best working mode (C_L=0p, I_{load} =20mA) and the worst working mode (C_L=100p, I_{load}=100uA), The phase margins of this LDO are 64° and 56.1° respectively, meeting the stability requirements.

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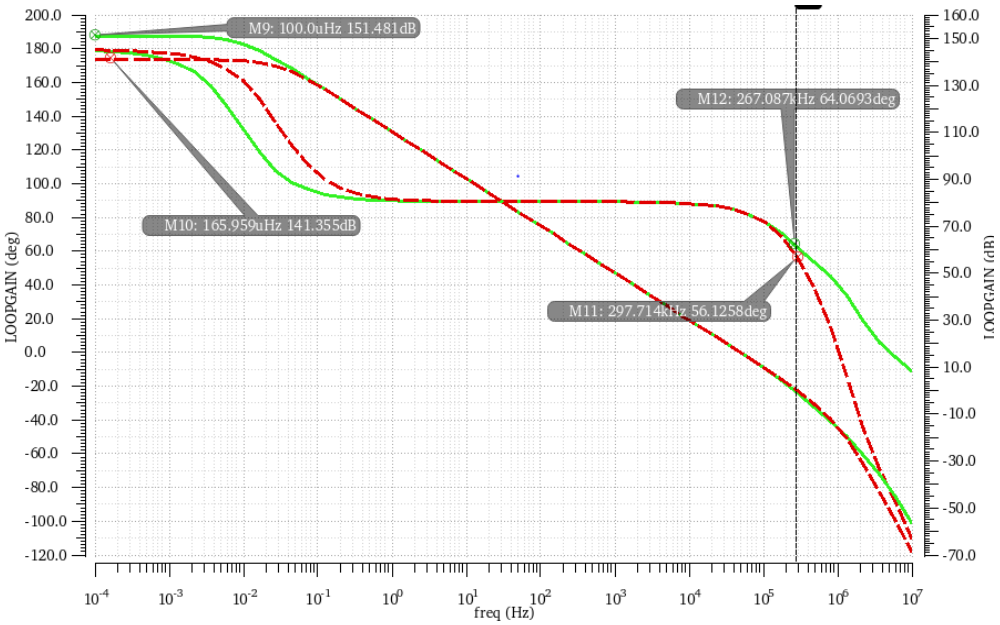

Fig.5 Stability simulation results

4. Concludion

This paper uses SMIC 0.13μm CMOS process to design an LDO with low power consumption and high transient response. By using two-stage error amplifier, nested miller compensation technology and slew rate enhancement circuit, it ensures good stability in various operating modes. At the same time, a low-power design is carried out. The quiescent current of this design is only 7.9μA, and the line regulation and load regulation are 0.047mV/V and 0.043mV/A, respectively. The LDO can maintain good stability under the load range of 100μA-20mA and the load capacitance of 0pF-100pF. The heavy-to-light-load settling time is 0.3μs, and the light-to-heavy-load settling time is 2.7 μs. The power supply rejection ratio (PSRR) is -44dB, the on-chip capacitance is 8.5pF, and the output voltage is 1.21V.

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