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Analysis and research of sigrity integrity in the DDR Full link simulation

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Abstract

Details of signal integrity in the circuits design is discussed in this paper, and the major influencing factors are analyzed such as ringing, reflection, bounce, crosstalk, also gives the principle of simultaneous switching noise and how to prevent them. Reflection can be reduced, through some proper measures of receiving termination while crosstalk can be mitigated via some measures, such as shortening the length of parallel line, increasing the line interval, adjusting the thickness of the medium layer, and supplying no cutting ground; SSN can be optimized via decreasing parallel lengths. Finally, we extract the full grounding and cutting grouding transmission line models using Ansys HFSS; then we simulate the singal integrity of full link DDR signals by Ansys Designer.

Keywords

Signal integrity; reflection; ringing; bounce; crosstalk.

1. Introduction

With the application of large-scale integrated circuits in system design, IC chips are becoming smaller and smaller, with more and more pins and higher working frequency. Engineers hope that the signals they care about are intact and undamaged when they arrive at the receiving end, but it often goes against their wishes. In today's increasingly high-speed digital system, it is becoming more and more difficult to generate and keep the signals intact. How to deal with the high-speed signal problem has become a key factor for the success of design. With the rapid increase of logic and system clock frequency and the steepening of signal edge in electronic system, the influence of trace interconnect and the characteristics of PCB layer on the electrical performance of the system becomes more and more important. Therefore, the design of high-speed systems must face timing problems caused by interconnect delay and signal integrity problems such as crosstalk and transmission line effect. Digital signal integrity has become an urgent issue for system developers [][1].

2. Concept of signal integrity and common problems:

Signal integrity (SI) refers to all abnormal voltage and current phenomena caused by the signal on the interconnect. The signal integrity problem is related to many factors, such as the increase of frequency, the decrease of rise time, the decrease of swing, the unsatisfactory interconnection channel, the bad power supply environment, the inconsistent delay between channels, etc., which may lead to the signal integrity problem, but its root is the relationship between channel transmission delay and signal rise time. On the one hand, the steep rising edge accentuates the problem of signal integrity. The root cause of the signal integrity problem lies in the increase of high-frequency components caused by the decrease of signal rise time, and many other influencing factors aggravate the signal integrity problem [][2].

Signal integrity problems mainly include reflection, ringing, ground projectile, crosstalk, synchronous switching noise and so on.

ISSN: 2664-9640

2.1. Reflection:

A mismatch in impedance between the source and the load causes on-line reflection, with the load reflecting part of the voltage back to the source, as shown in Figure 1. If the load impedance is less than the source impedance, the reflected voltage is negative; Conversely, if the load impedance is greater than the source impedance, the reflected voltage is positive. Variations in wiring geometry, incorrect wire terminations, transmission through connectors, and discontinuities in the power plane can cause such reflections.

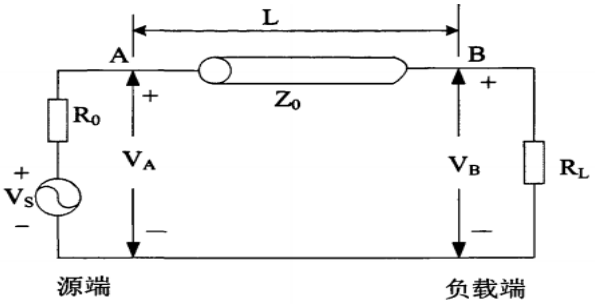

Figure 1 Reflection schematic diagram

2.2. Ring:

Ringing of signals refers to the excessive inductance and capacitance on the line. The signals may fluctuate up and down at high and low levels. Ringing will make the signal threshold fuzzy and also easily cause EMI, as shown in FIG. 2. Ringing, like reflection, can be caused by a variety of factors, and can be reduced by appropriate endpoints, but cannot be completely eliminated.

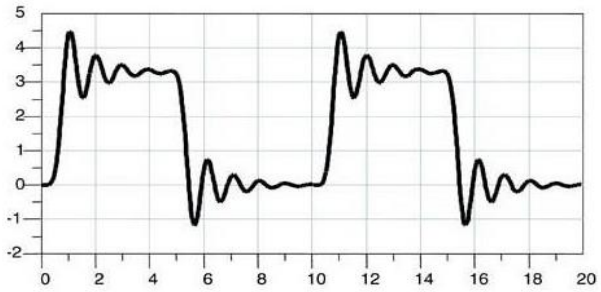

Figure 2 Ringing waveform

2.3. To play:

Circuit has a great surge of electric current will cause the bomb, such as a large amount of chip output at the same time open, there will be a larger transient current flow in the chip from the power source of the plate plane, chip packages and resistance and inductance of the power plane will cause the power supply noise, this will produce the voltage fluctuation on the real ground plane and change, the noise will affect other components of the action, See Figure 3. The increase of load capacitance, load resistance, ground inductance and the number of switching devices will lead to the increase of ground missile.

2.4. Crosstalk:

Crosstalk is the coupling between two signal lines. The mutual inductance and tolerance between signal lines cause the noise on the line. When two signals are close to each other, the electromagnetic field of one signal will cover the other signal, thus introducing crosstalk on the other signal. Crosstalk can be divided into three forms: interwired crosstalk, loop crosstalk and plane crosstalk (commonly seen in digital-analog hybrid circuit), as shown in Figure 4. Capacitive coupling initiates a coupling current, while inductive coupling initiates a coupling

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voltage. The parameters of PCB board layer, the distance between signal lines, the electrical characteristics of driving end and receiving end and the connection mode of line all have certain influence on crosstalk. Both ringing and ground shot belong to the phenomenon of single signal line (accompanied by ground plane loop) in signal integrity problems, while crosstalk is caused by two signal lines and ground plane on the same PCB board, so it is also called three-wire system.

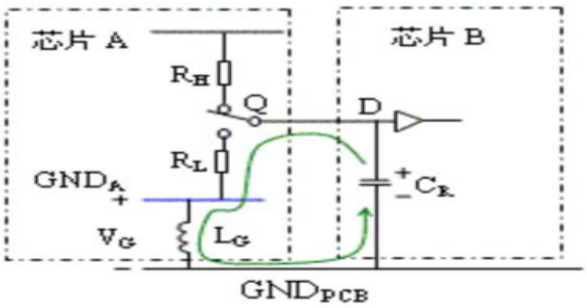


Figure 3 Schematic diagram of ground missile

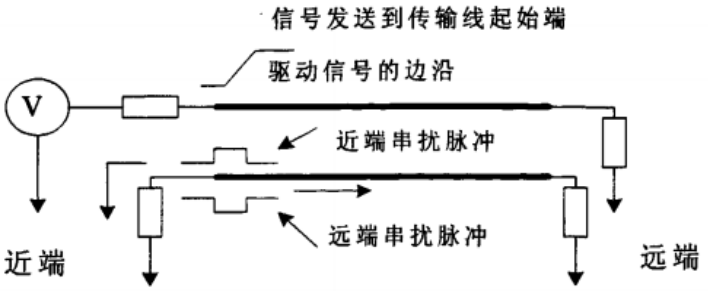


FIG. 4 Schematic diagram of crosstalk

2.5. Synchronous switching noise:

Synchronous switching noise refers to the noise caused by ac voltage drop when the device is in the switching state and the current that changes instantaneously passes through the inductance existing in the backflow path. See Fig.5. If it is due to the package inductance caused by the ground plane fluctuation, resulting in chip and system inconsistent, this phenomenon is called ground elastic. Similarly, if the chip and system power difference is due to package inductance, it is called power rebound. Therefore, the synchronous switching noise is not completely the problem of power supply, and its influence on power supply integrity is mainly manifested as the ground/power rebound phenomenon.

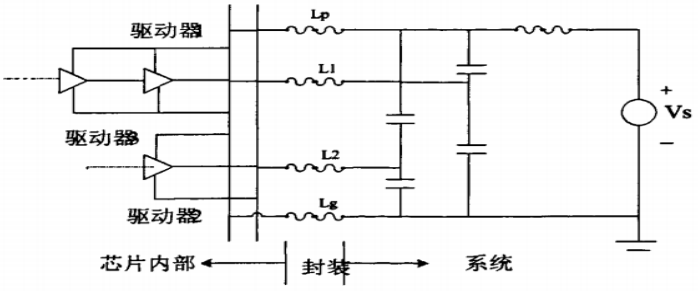


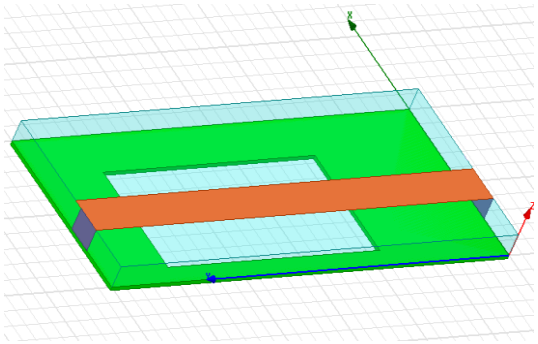
FIG. 5 Schematic diagram of synchronous switching noise

ISSN: 2664-9640

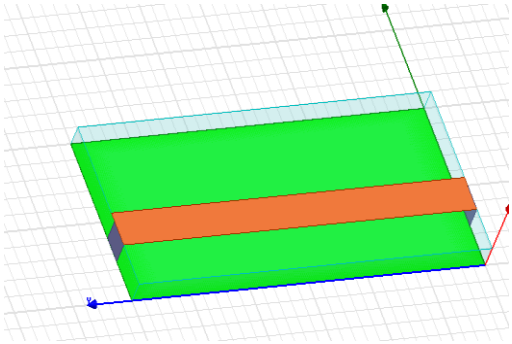
3. Influence of backflow segmentation on signal integrity:

3.1. Reflection simulation analysis:

For back-flow segmentation reflection simulation, electromagnetic field simulation software is used to simulate reflection and transmission characteristics of 50ohm microstrip transmission line on PCB, as shown in Figure 6 below. FIG. 6 (a) and FIG. 6 (b) are reflection simulation models of reflux ground plane segmentation and complete reflux ground plane respectively.



(a) Backflow segmentation reflection simulation model diagram



(b) Complete reflow ground plane reflection simulation model diagram

FIG. 6 Simulation model diagram of reflux ground segmentation and complete reflux ground plane reflection

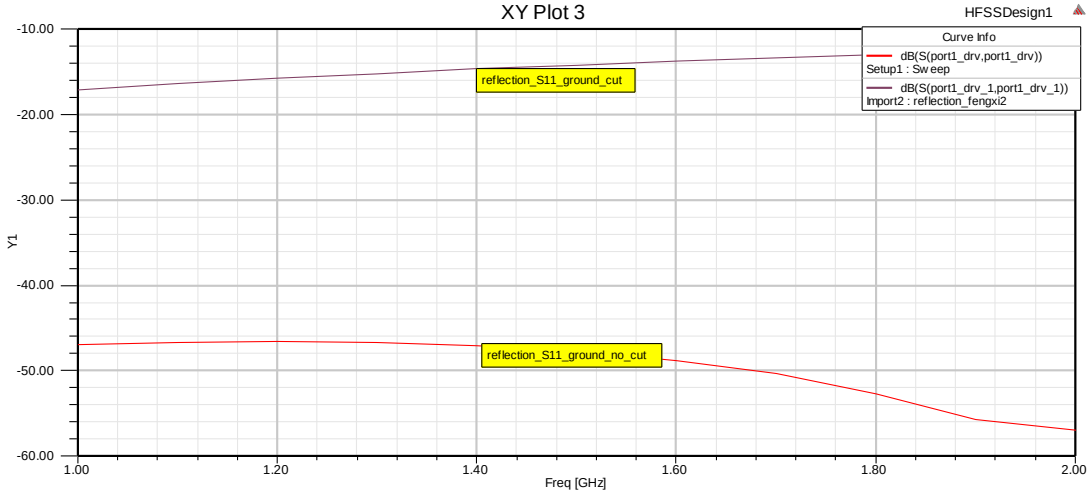


FIG. 7 Comparison of S11 reflection parameters between reflux ground segmentation and complete reflux ground plane

FIG. 7 and FIG. 8 show the simulation comparison results of S11 reflection parameters and S21 parameters obtained from the backflow ground segmentation and the complete backflow ground plane from the simulation model in FIG. 6. Compared with the S11 reflection parameters of the complete backflow ground plane (FIG. 7, red line), the simulation results of backflow ground segmentation (FIG. 7, purple line) are optimized by 30dB at 1GHz. Compared with S21

ISSN: 2664-9640

transmission parameters with complete backflow ground plane (FIG. 8, red line), the simulation results with backflow ground segmentation (FIG. 8, purple line) are optimized by 0.2dB at 1GHz.

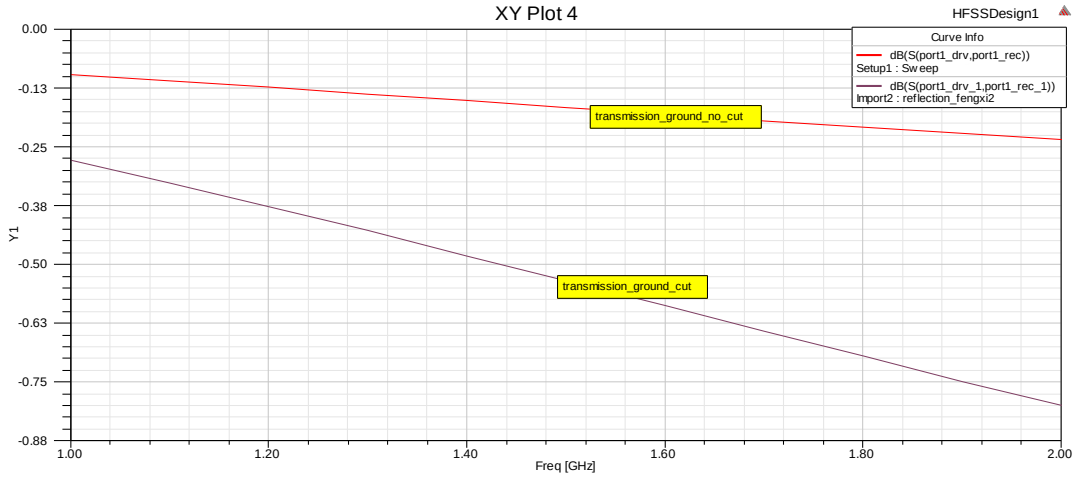
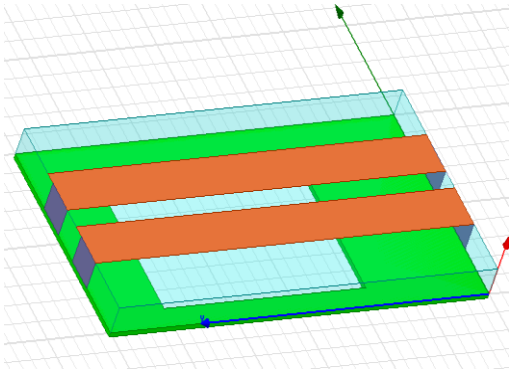


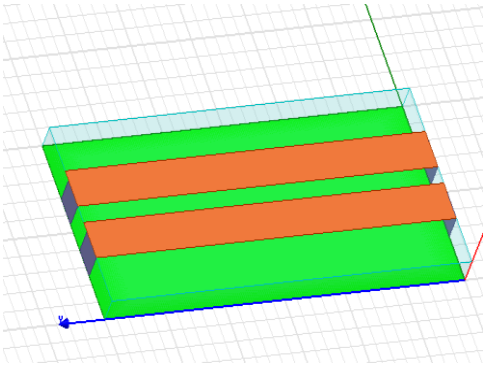
FIG. 8 Comparison of S21 transmission parameters between reflux ground segmentation and complete reflux ground plane

3.2. Crosstalk simulation analysis:

Crosstalk is very common in digital design, and exists on PCB boards, connectors, chip packages, and connector cables. Too much crosstalk may cause the circuit to be triggered by mistake and the system cannot work properly. In actual PCB design, crosstalk is closely related to line length, line spacing and reference ground plane. Here, the influence of backflow ground segmentation on crosstalk is analyzed through simulation. FIG. 9 (a) and (b) are the simulation models of backflow ground segmentation and complete backflow ground plane crosstalk respectively.



(a) Backflow segmentation crosstalk simulation model diagram



(b) Complete backflow plane crosstalk simulation model diagram

FIG. 9 Simulation model diagram of backflow ground segmentation and complete backflow ground plane crosstalk

ISSN: 2664-9640

Simulation comparison of near-end and far-end crosstalk obtained from the simulation model in FIG. 9 is shown in FIG. 10 and FIG. 11 respectively. The simulation results of the near-end cross-talk with the complete s-parameter of back-flow ground plane (FIG. 10, red line) were compared with the simulation results of back-flow ground segmentation (FIG. 10, purple line), which were optimized by 4dB at 1GHz. The simulation results of remote crosstalk with complete backflow ground plane (FIG. 11, red line) were compared with that of backflow ground segmentation (FIG. 11, purple line), which optimized 7dB at 1GHz.

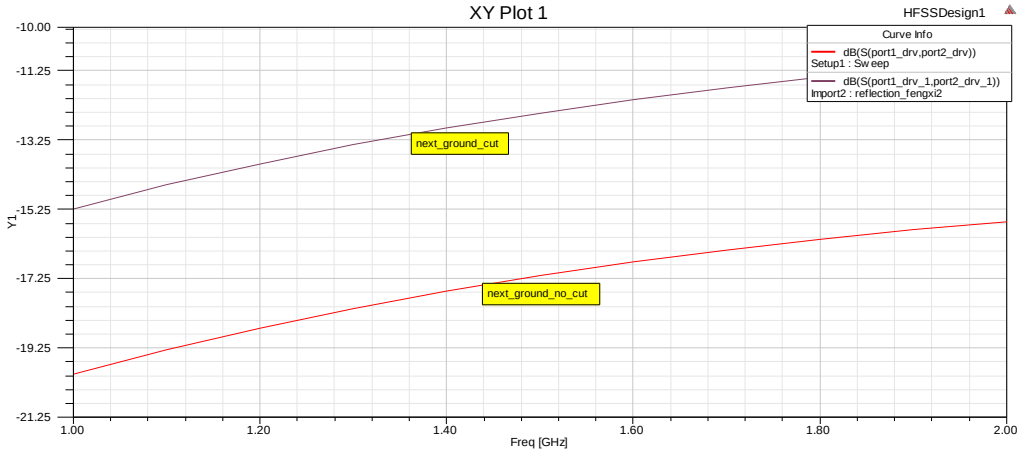


FIG. 10 Comparison of near-end crosstalk S parameter between reflux ground segmentation and complete reflux ground plane

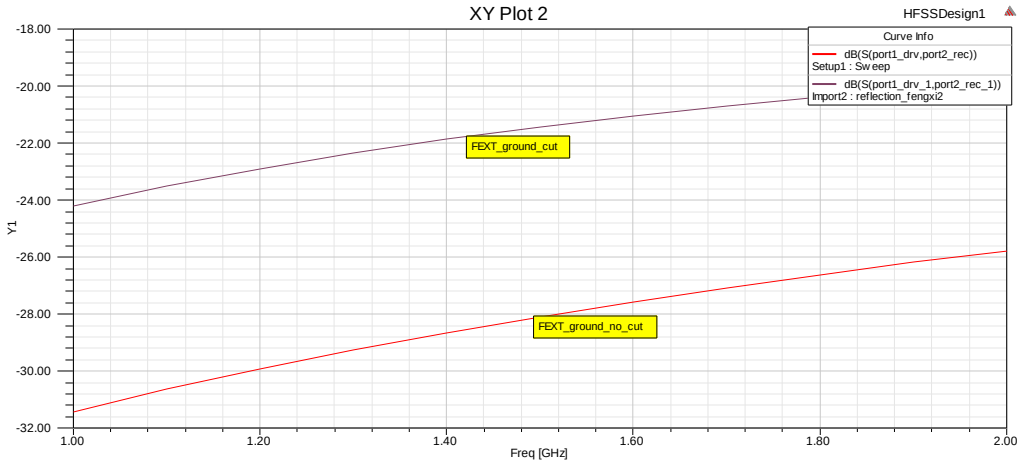


FIG. 11 Comparison of remote crosstalk S parameters between backflow ground segmentation and complete backflow ground plane

3.3. Analysis of simulation results:

Return to segmentation will increase the reflection of PCB microstrip line, the transmission performance of microstrip line, reduce PCB increase between adjacent line near end crosstalk and far end crosstalk, so in the real PCB design, high speed, simulation or other key signal of walk line below to obligate full back ground plane, so as to improve the quality of critical path signal of the signal, Ensure stable transmission of high-speed, analog and other key link signals.

4. Conclusion

As high-speed electronic designs become more common, signal integrity problems will become more apparent. This paper introduces the common problems of PCB signal integrity and the

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effect of backflow segmentation on signal reflection and crosstalk. It can be predicted that with the continuous improvement and improvement of signal integrity analysis model and computational analysis algorithm, design methods based on signal integrity analysis will be more and more applied in electronic product design [[3]]. However, in China, due to the limitations of technology and capital conditions, it has not been widely used, so it is urgent to learn and improve conditions, in order to improve the design level, enhance the competitiveness of products.

References

[1] Yu Bo, et al. Signal Integrity Design for High-speed Electronic Circuits [J]. Journal of Beijing Institute of Technology, 1999, 31 (4): 3- 7.

[2] Mao Zhongyu, et al. Simulation design of signal and power supply integrity and application examples of high-speed products. Publishing House of Electronics Industry.2018 .

[3] Zhang Bo,Zhang Huanchun,Jing Yazhi, et al. Design technology of High-speed Digital Circuit System Based on SHARC [J]. Semiconductor technology, 2002, 27 (2): 50- 53.