ISSN: 2664-9640

Design of SFP28 test and debugging evaluation board

Junhan Wang, Yaxiong Gu

School of mechanical and electrical engineering, Southwest Petroleum University, Sichuan 610000, China;

Abstract

This paper mainly designs and develops an evaluation board for testing and debugging SFP28 optical module. The evaluation board can test the optical eye diagram, electric eye diagram, optical power, wavelength, sensitivity and power consumption of SFP28 module at the same time, and test the performance of receiving end and transmitting end of SFP28 module together. At the same time, the evaluation board can read the internal register information of SFP28 module and the real-time monitoring of DDMI. It can modify the internal register information of the module, configure the look-up table and other operations through software, and debug the relevant performance of the module according to the feedback of the test situation and the real-time monitoring of SFP28 module. The evaluation board can greatly improve the testing efficiency of SFP28 module, and then improve the production efficiency of the module.

Keywords

SFP28; Optical module; Testing; Commissioning; Evaluation board.

1. Introduction

With the rapid development of communication technology in China and the technological innovation of mobile communication for ten years, 5G communication has become a hot topic. 5G communication requires a peak rate of 10 to 20Gbit / s. The demand for SFP+ (10G rate) and SFP28 (25G rate) optical modules is increasing. At the same time, people's performance requirements for optical modules are also gradually improving. In this context, the low cost and high efficiency of testing and debugging optical module performance platform have attracted more and more attention, which will greatly affect the production quality, production efficiency and production cost of optical module.

The main indexes to evaluate the performance of optical module include optical power at the transmitting end, optical eye diagram, wavelength, electric eye diagram at the receiving end, sensitivity, overload point and power consumption of optical module. When testing the eye diagram of the optical module, it is necessary to use an external signal source to send pseudo-random code and clock signal to the optical module. When testing the receiving sensitivity of the optical module, the signal received by the receiving end of the optical module needs to be compared with the signal sent by the signal source to calculate the bit error rate. The bit error rate within a certain time is the main index used to measure the receiving sensitivity of the optical module. In order to meet the test requirements of optical module, a signal generator that can generate pseudo-random code and clock signal is needed, and the bit error meter is born as the signal source.

At present, foreign BER products have relatively good performance and high speed of testable signal, but the price is relatively expensive and the maintenance is relatively troublesome; In China, with the vigorous development of optical communication, although there are many bit error meters with relatively low price in the market, most of these products have various defects, such as low rate of testable signal, few choice of communication interface and so on. Therefore, most domestic optical module manufacturing enterprises can only choose to

ISSN: 2664-9640

purchase bit error meter from abroad at a high price, which greatly increases the manufacturing cost of optical module and limits the promotion of high-speed optical module in the market to a certain extent.

In addition, the bit error meter can not fully meet the test requirements of the optical module, and can not test all the indicators required to evaluate the performance of the optical module. When testing the electric eye diagram of the receiving end of the optical module and the power consumption of the optical module, other test circuits need to be designed. Therefore, the test of the optical module cannot be in place at one time, and the test circuit and equipment need to be replaced back and forth in the test process, which leads to the failure to improve the test efficiency of the optical module, thus affecting the production efficiency of the optical module.

In order to solve these problems, this paper designs a low-cost evaluation board for testing and debugging SFP28 optical module. The evaluation board has the function of bit error meter, which can generate pseudo-random code and send it to SFP28 optical module to test the optical eye diagram and sensitivity of the module. Moreover, the evaluation board also has the hardware circuit required to test the power consumption and other performance of the module, which can meet the requirements of simultaneous testing at both ends of SFP28 module. At the same time, the evaluation board can debug the performance of SFP28 module through software control, so as to improve the test efficiency of optical module to a certain extent and reduce the manufacturing cost of domestic optical communication industry.

2. Test principle

The test schematic diagram of SFP28 module transceiver is shown in Figure 1 :

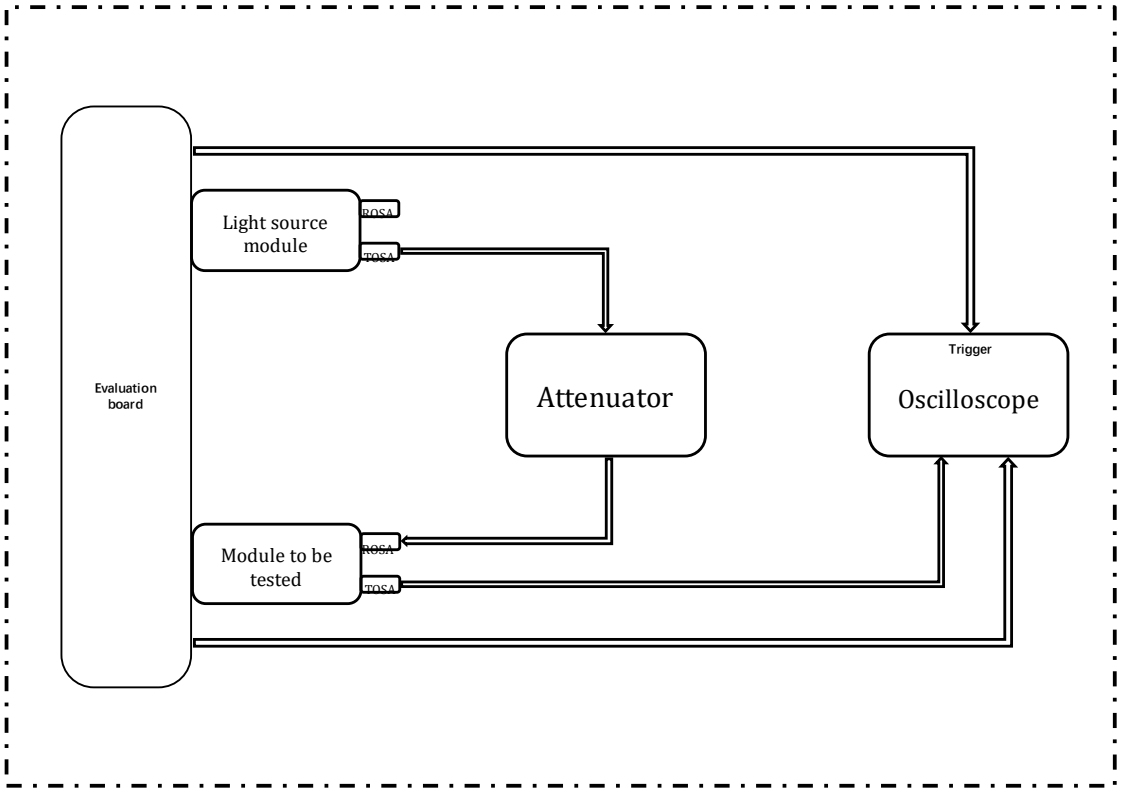

Fig. 1 Test principle of SFP28 module

When testing SFP28 module, first lead out the clock signal of the evaluation board to the trigger interface of the oscilloscope to provide synchronous clock signal for the oscilloscope for the optical and electrical eye diagram of subsequent test modules. When testing the performance of the module, insert the module to be tested into the evaluation board, and connect the TOSA

ISSN: 2664-9640

end of the module to the optical port of the oscilloscope with optical fiber, so as to test the optical eye diagram of the module. When testing the performance of the receiving end of the module, connect the TOSA over attenuator of the light source module to the ROSA of the module to be tested, and gradually increase the attenuation of the attenuator. The minimum light that the ROSA end of the module to be tested can receive without packet loss (if the bit error rate is less than 10E-12 within the specified time, it is considered as no packet loss) is the sensitivity of the module to be tested. Connect the electrical signal at the receiving end of the module to be tested to the electric port of the oscilloscope for testing the electric eye diagram of the module. When testing the SFP28 module whose modulation signal comes from an external signal source, such as a switch, it is necessary to extract the clock signal of the external signal source and connect it to the oscilloscope to test the eye diagram of the module. The specific principle is shown in Figure 2:

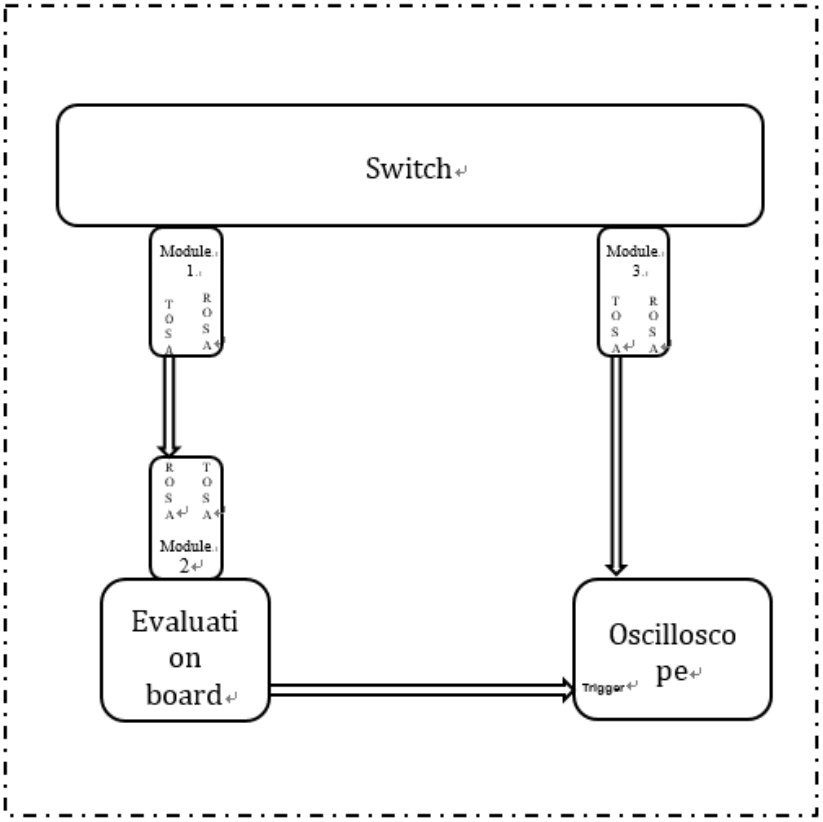

Fig. 2 Test principle of external signal source module

Insert module 1 to the switch and module 2 to the evaluation board. These two modules help extract the synchronization clock of the switch. Connect the sending end of module 1 to the receiving end of module 2, convert the modulated electrical signal from the switch into optical signal through module 1, transmit it to module 2 through optical fiber, and then convert the return signal through module 2. The electrical signal extracts the clock signal through the receiving CDR circuit on the evaluation board, and leads the clock signal to the trigger port of the oscilloscope to provide the oscilloscope with the clock signal synchronized with the switch. Then insert the module 3 to be tested into the switch and connect the optical port of the oscilloscope with optical fiber to test the module eye diagram.

ISSN: 2664-9640

3. Hardware implementation

Compared with SFP+ module, the communication rate of SFP28 is increased from 10Gbit / s to 25Gbit / s. not only the manufacturing technology of optical module needs to be improved, but also the design of hardware circuit of test optical module needs to be further improved. In order to improve the quality of the optical eye diagram of the sending end and the electrical eye diagram of the receiving end of the SFP28 module, reduce the interference caused by the test circuit, and more accurately measure the sensitivity of the receiving end of the module, CDR (clock data recovery) circuit needs to be added at the sending and receiving ends of the corresponding module in the test circuit. The hardware design diagram of the test and debugging evaluation board is shown in Figure 3 :

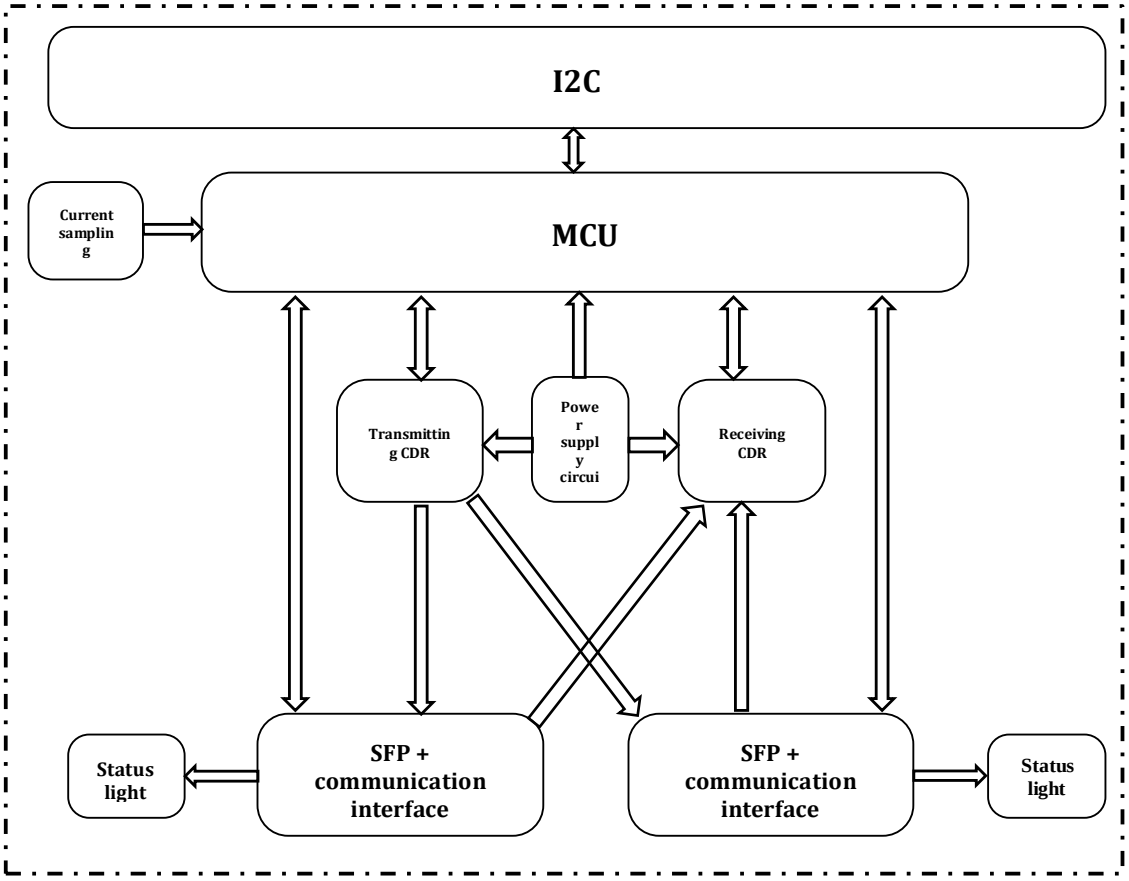

Fig. 3 Hardware design diagram of evaluation board

The hardware circuit of the test, debugging and evaluation board is mainly composed of I2C bus, power supply circuit, MCU, receiving CDR circuit, transmitting CDR circuit, current sampling circuit, SFP+ communication interface and status light.

I2C bus is a two-way two-wire synchronous serial bus, which is led out by the transfer chip CH341A of USB bus. It is the main communication line in the circuit of this evaluation board, which is connected with MCU to realize the information exchange with the upper computer. The upper computer realizes software control of MCU through I2C bus, and obtains relevant information in the whole test process from MCU.

The power supply circuit is the main supply source in the circuit of this evaluation board, which is compatible with USB and external DC power supply. LT1963 chip adjusts the external input voltage of 4.5V to 3.3V, and stabilizes and filters to supply power to MCU. APD5034 chip filters and adjusts the voltage of 3.3V to 1.6V, and supplies power to the CDR circuit of the receiving end and the transmitting end respectively in two ways.

ISSN: 2664-9640

MCU is the control core in the circuit of this evaluation board. It uses DS4830A chip to control the operation of the whole circuit. The upper computer can send instructions to CDR chip through MCU to generate pseudo-random code and clock signal for testing various performance indexes of the module. The sampling information of the current sampling chip is transmitted to the host computer through MCU, so as to obtain various parameters in the test process, and then calculate the power consumption of SFP28 module. MCU is directly connected with SFP+ interface to obtain the internal register information of the module and the real-time monitoring of DDMI. The upper computer can change the internal register of the module, configure the look-up table and control the relevant functions of each chip in the module through MCU, so as to achieve the purpose of debugging the module.

The CDR circuits at the receiving and transmitting ends are mainly developed around the CDR chip GN2104S. The CDR circuit of the originator is the signal source of the evaluation board. The pseudo-random code and clock signal generated by MCU are transmitted to the SFP+ interface, and transmitted to the module through the SFP+ interface as the modulation signal of the module. At the same time, a clock signal can be led out and transmitted to the oscilloscope to test the eye diagram of the module.

After receiving the light, the module converts the optical signal into an electrical signal and transmits it to the receiving CDR circuit through the SFP+ interface. The receiving CDR circuit compares the received pseudo-random code signal with the transmitted pseudo-random code signal, calculates the number of error codes and stores them in the chip. The upper computer reads out the number of bit errors through MCU and calculates the bit error rate in the transmission time period, which is used to evaluate the sensitivity of SFP28 module. At the same time, the received signal can extract a channel of clock signal through clock recovery and transmit it to the oscilloscope for testing the eye diagram of the module using other signal sources as modulation signals.

The current sampling during the operation of the evaluation board is completed by MAX4378FAUD chip, which is a high-precision current sensing amplifier. The current can be accurately read out by selecting appropriate voltage gain and external induction resistance. The current sampling circuit composed of chip MAX4378FAUD is used to sample the working current of SFP28 module, so as to calculate the power consumption of the module and feed it back to the host computer through MCU.

In the circuit of this evaluation board, the communication interface with SFP28 module adopts the communication interface of ordinary SFP+ module. Since the design of SFP28 module complies with SFF-8431 protocol, the definitions of each pin in the golden finger of SFP28 module are the same as that of SFP+ module, so the communication interface of SFP28 module can be consistent with that of SFP+ module.

The status light is composed of six light-emitting diodes, which are respectively connected with each pin of SFP+, and is used for the in position status of the range module. When the module is not inserted, the diode is in the light-emitting state. When the module is inserted, the status light goes out. If the status of the module is abnormal, the corresponding status light will not go out.

4. Software implementation

When testing and debugging SFP28 module, in order to improve production efficiency, the upper computer controls the implementation of testing and debugging through software. The specific software control process is shown in Figure 4:

ISSN: 2664-9640

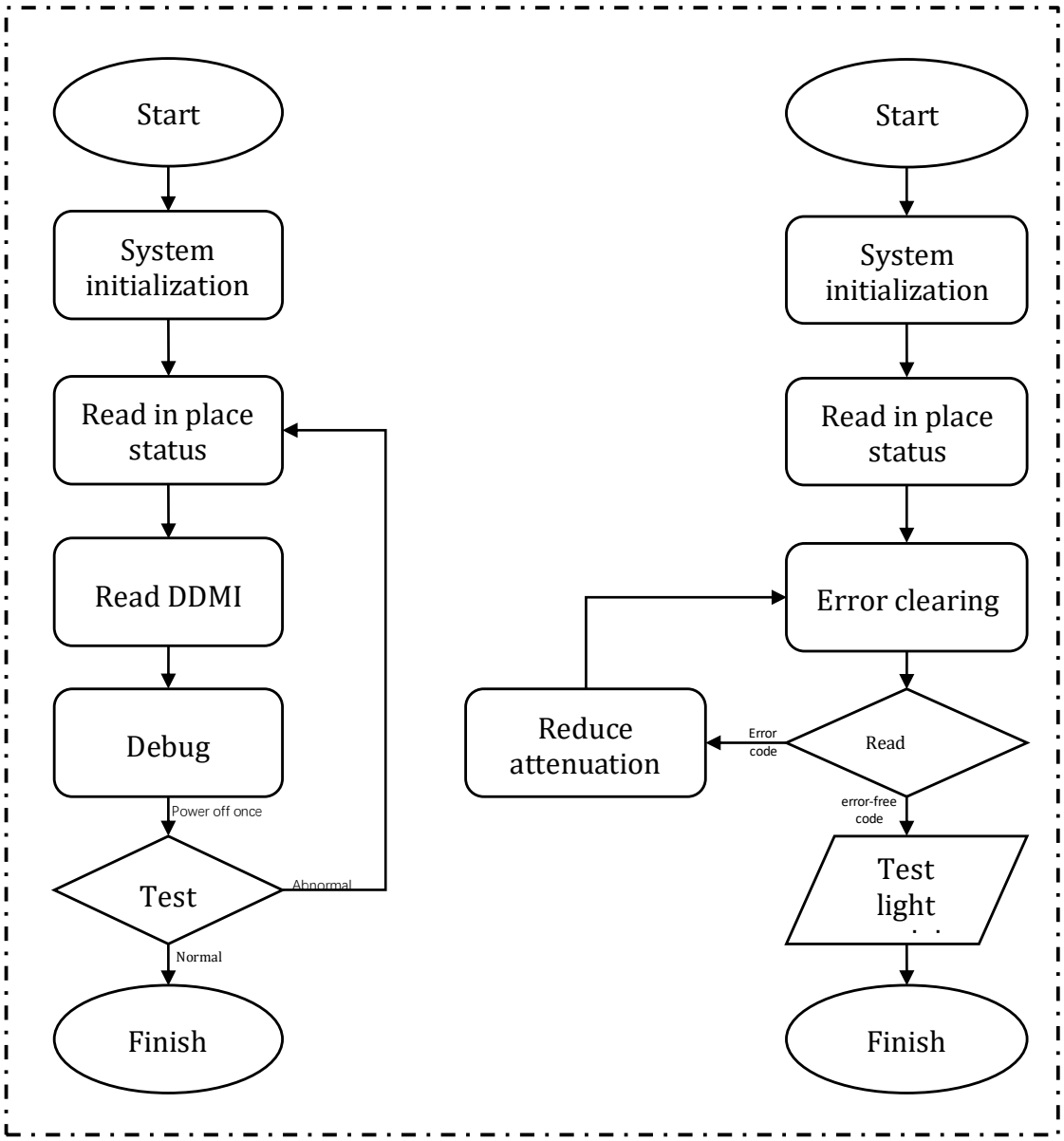

Fig. 4 Software control flow chart

The production of SFP28 module shall be debugged first, and the module shall be debugged until the function is normal before testing. Debugging is generally conducted for the sending end of SFP28 module, and the receiving end can be tested directly after register configuration. The left side of Figure 4 shows the process of debugging and testing the originator of SFP28 module. First, initialize the system, MCU enables the CDR circuit at the sending end to send a signal, and the evaluation board starts to work. Then read the module in place status signal and check whether the module is in place. Read the DDMI monitoring module and start debugging. After the module debugging is completed, power off once to ensure that the internal register of the module is changed successfully and the module debugging is successful. Test the performance of the module originator. If the originator is normal, it ends. If the originator is abnormal, re test the module in place and debug again until the test passes.

The right side of Figure 4 shows the sensitivity test process of SFP28 receiver. First initialize the system, MCU enables the CDR circuit of the transmitter to send a signal, sets the attenuation value of the attenuator to the maximum, and then clears the number of error bits stored in the CDR circuit chip of the receiver to prepare for the test. Detect the module in place status signal. After confirming that the module is in place, the software starts timing and reads the number

ISSN: 2664-9640

of errors, and then calculates the bit error rate during this period. If there is any error code (i.e. the bit error rate is greater than 10E-12), reduce the attenuation value of the attenuator, clear the error code and test again. Read the error free code (i.e. the bit error rate is less than 10E-12) until 90 seconds of the test, and then test the actual optical receiving power at the receiving end of the module, which is the sensitivity of the module.

Summary

The evaluation board designed in this paper can be used to test and debug the performance of SFP28 module. The tests at both sending and receiving ends of the module are carried out at the same time, which greatly simplifies the production process of SFP28 module, improves the production efficiency of SFP28 module, reduces the production cost, and promotes the development process of SFP28 module to a certain extent.

References

[1] Zhou Yang, Xiong Junqiao Design and optimization of 10Gbit / s SFP+ optical module test platform [J] Measurement and control technology, 2022,41 (02): 64-69.
[2] Wang Huitao, Zhang Pinghua, Su Zhan 800Gbit / s optical module technology and application [J] ZTE Technology: 1-14.
[3] Wang Zhihao Research on basic component technology of SFP optical communication module [D] Beijing Jiaotong University, 2020.
[4] Ye Feng, Hu Zhengxin Research and design of 25G SFP28 CWDM optical module technology [J] Information and communication, 2020, (05): 62-63.
[5] Zhou Lu, Wu Keyu Research on SFP+ sensitivity test scheme [J] Electronic design engineering, 2020,28 (06): 107-110.
[6] Zhao Guanbao Research and implementation of a low cost and high reliability SFP+ optical transceiver module circuit [J] Modern transmission, 2019, (04): 51-54.
[7] Sun Xiaoqiang Design of multi-channel and multi rate bit error meter in optical fiber communication [D] Harbin Institute of technology, 2018.
[8] Hu Jintao, Sun Liping, Wang Jing 25Gbit/s SFP+ the first mock exam module of [J]. technology. Optical communication research, 2017, (02): 54-57.
[9] Zhang Chu Design of low cost 4 * 25G multichannel parallel bit error meter [D] Huazhong University of science and technology, 2017.
[10] Xiong Feng Design and implemen.tation of SFP optical module automatic test system [D] Wuhan University of technology, 2015.
[11] Zhou Fengjin Research and implementation of SFP optical module monitoring system [D] Wuhan University of technology, 2012.
[12] Zhou Zhiyong, Zhang Liuyu, Gao Fanrong, Xu Hongchun Design and development of 10Gb / s error code discussion [J] Optical communication technology, 2011,35 (02): 22-24.
[13] Hu Cihui Hardware circuit design and implementation of high speed bit error test system based on FPGA [D] Wuhan University of technology, 2010.
[14] Zhou Jinlin Design and implementation of optical transceiver module monitoring system [D] Beijing University of Posts and telecommunications, 2010.
[15] Hu Jiming, Zhang Xiaolin, Feng Wenquan Design and implementation of programmable bit error meter [J] Electronic measurement technology, 2006, (05): 112-114.