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Design of Synaptic Circuit Based on STDP Learning Rules

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Abstract

Based on 65nm CMOS process, this paper designs a low-power, energy-efficient and compact synaptic circuit that can be used in spiking neural network systems. The synaptic circuit adopts the switched capacitor circuit structure, directly receives the pulse signal from the neuron circuit, and adjusts the synaptic weight in real time according to the learning rule of Spike-Timing Dependent Plasticity (STDP). The synaptic circuit mainly includes a control switch, a signal attenuation circuit, a weight update circuit, and so on. The weight update circuit adopts a voltage divider structure, and the voltage value of synaptic weight is changed by changing the input voltage of voltage divider, wherein the synaptic weight voltage is stored in the capacitor.

Keywords

CMOS; Spiking neural network; STDP.

1. Introduction

The spiking neural network is a machine learning method based on the human brain to improve the ability and energy efficiency of machine learning. Using knowledge of neuroanatomy, spiking neural networks approach the energy efficiency limit of biological systems by means of temporally sparse spiking communication, spatially sparse connections, reduced precision, and approximate computation. Using neurophysiological knowledge, the intelligence of the brain can be simulated through temporal pulse encoding and biologically trusted learning [1]. In the biological nervous system, the special part where neurons and neurons or between neurons and non-nerve cells (such as muscle cells or gland cells) contact each other and realize signal transmission is called synapse, which is the connection and communication between neurons. A key structure for carrying out physiological activities [2].

The synapse is used to adjust the connection strength between any two neurons in the nervous system. The connection strength of the synapse is also called the synapse weight. The larger the synapse weight, the stronger the connection strength between the two neurons, and vice versa. The smaller the synaptic weight, the weaker the connection strength. Learning in the brain can be understood as a process of changing the strength of synaptic connections over time, this capability called synaptic plasticity. For the simulation of synaptic plasticity, the widely used learning rule is the Spike-Timing Dependent Plasticity (STDP) learning rule. Timing will lead to different synaptic change processes, and the result of synaptic weight changes can be expressed as a function of the time difference between pre- and post-synaptic spikes, called the learning window.

By implementing the update rules of the synaptic weights in the hardware circuit, the nervous system can be made to respond faster, without the need to process the pulse signal through an external device, nor to store the pulse time difference. Reference [3] uses an analog circuit to implement a synaptic circuit according to the STDP learning rule, but the time window shape of the simulated STDP rule does not show an exponential decay in a strict sense. Reference [4] implements the exponential STDP learning rule, and the energy consumption is as low as 0.4 pJ/spike, but the implementation of its circuit includes 5 transconductance amplifiers, and the

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circuit requires additional auxiliary circuits such as bypass capacitors and output buffers. The circuit structure is more complicated. Reference [5] implements a tunable STDP learning rule, but the circuit consumes 23 nJ and 1 μJ each time the synaptic weight is decreased and increased, respectively, and the power consumption is high.

Based on the 65nm CMOS process, this paper proposes a low-power, compact synaptic circuit, which realizes the STDP learning window for synaptic weight update, and can be matched with analog neuron circuits. The circuit structure is simple and the number of transistors is small, which is suitable for large-scale integration.

The organization of this paper is as follows. Section 2 mainly introduces the STDP learning rules of synaptic circuits; Section 3 introduces the structural design of the synaptic circuits; Section 4 introduces circuit simulation and test results; Section 5 gives conclusions.

2. Spike-Timing Dependent Plasticity

Neuroscience studies have found that the way of encoding pulse frequency cannot fully represent the actual role of synaptic plasticity, and the changes of synaptic weights are closely related to the precise timing of neuron firing [6]. The relative time difference between presynaptic and post-synaptic pulses plays a key role in the direction and size of synapses between neurons. This learning rule based on the timing of pre- and post-synaptic pulses is called STDP [7] learning rule. In this paper, the STDP learning rule is used to design the synaptic circuit.

Assuming that there is a neural connection W_{ij} from the presynaptic neuron i to the postsynaptic neuron j, the STDP learning rule is expressed as: 1) If the postsynaptic neuron j generates a response and emits a pulse after the pulse emitted by the presynaptic neuron i reaches the synapse, the synaptic weight W_{ij} between neurons will increase; 2) If postsynaptic neuron j sends a pulse before pre-synaptic neuron i transmits a pulse, then this information may be ignored, the synaptic weight W_{ij} between neurons will weaken. If the time difference is too large, the synaptic weights will not change.

The above STDP learning rule can be represented by an exponential function:

$$\Delta W(s) = \begin{cases} +A_+ \exp(-\frac{s}{\tau_+}), s \geq 0 \\ -A_- \exp(\frac{s}{\tau_-}), s < 0 \end{cases} \quad (1)$$

In the formula (1), $\Delta W(s)$ represents the change value of the synaptic weight, the parameters A_+, A_-, τ_+, τ_- control the shape of the STDP learning window, and s represents the output pulse time difference between the postsynaptic neuron and the presynaptic neuron. This function is also called the STDP learning window of the synapse [8], and its change trend is shown in Fig. 1. The abscissa $s = t_{post} - t_{pre}$ corresponds to the time difference s in equation (1), and the ordinate corresponds to the time difference ΔW in equation (1). A_+ and A_- represent the maximum value of synaptic weight increase or decrease, respectively, and τ_+ and τ_- represent the time constant of synaptic weight increase or decrease, respectively.

3. Circuit architecture of synapse

Based on STDP learning rules, this paper designs a synaptic circuit structure. The synaptic circuit receives the pulse signals output by the neurons before and after the synapse, and converts the time difference between the two pulse signals into the change of the synaptic weight. The learning window for synaptic weight changes is shown in Fig. 1.

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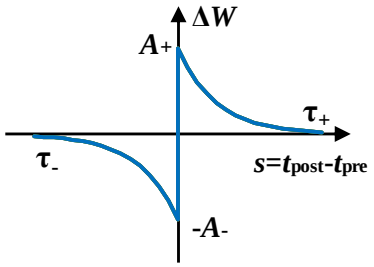

Fig. 1 Synaptic weight learning window

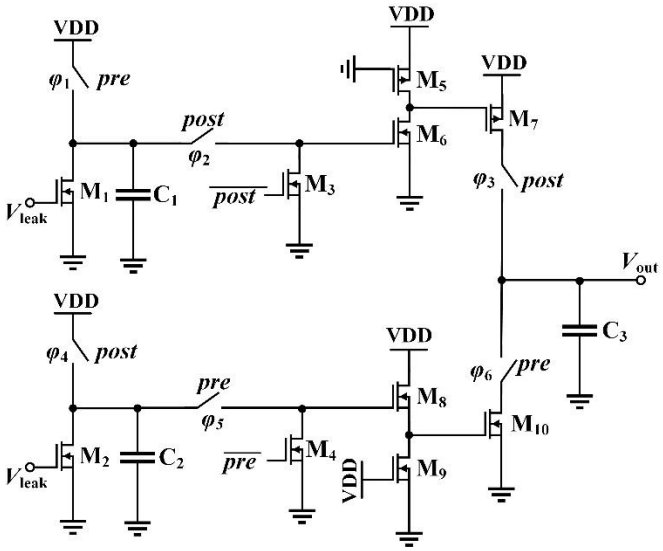

Fig. 2 The schematic of synaptic circuit proposed in this paper

The synaptic circuit adopts a switched capacitor circuit structure, and the schematic diagram is shown in Fig. 2. The synaptic circuit includes two parts of circuits with symmetrical upper and lower structures, each part of the circuit includes: a control switch, a signal attenuation circuit and a weight update circuit, wherein the input end of the signal attenuation circuit of the upper part of the circuit is connected with the control switch φ_1. The attenuation circuit and the weight update circuit are connected through the control switch φ_2. The input end of the signal attenuation circuit of the lower half circuit is connected with the control switch φ_4, and the signal attenuation circuit and the weight update circuit are connected through the control switch φ_5. The weight update circuit changes the charge stored on the capacitor C_3 by charging and discharging the capacitor C_3, thereby changing the value of the synaptic weight voltage.

The signal attenuation circuit of the upper half of the synapse circuit is composed of NMOS transistor M_1 and capacitor C_1. When the external pulse signal *pre* arrives, the control switch φ_1 is turned on, and the capacitor C_1 is charged to VDD. With the end of the external pulse signal *pre*, the capacitor C_1 is discharged, and the voltage across the capacitor C_1 decays exponentially. The control switch φ_2 is used to transmit the voltage at both ends of the capacitor C_1 that decays to the arrival of the external pulse signal *post* to the NMOS transistor M_6. NMOS transistor M_6, PMOS transistor M_5 and PMOS transistor M_7 constitute a weight update circuit, which is used to convert the voltage signal transmitted through the control switch φ_2 into a current signal, and transmit it to the capacitor C_3 through the control switch φ_3 to charge the capacitor C_3, so as to realize the increase of the synaptic weight when the postsynaptic pulse signal *post* reaches the synaptic circuit after the presynaptic pulse signal *pre*. The NMOS transistor M_3 is controlled by the opposite signal of the external pulse signal *post*. When there is no external pulse signal

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post input, the NMOS transistor M_3 pulls down the gate voltage of the NMOS transistor M_6 to GND to avoid static power dissipation in the circuit when there is no signal control.

The signal attenuation circuit of the lower part of the circuit is composed of NMOS transistor M_2 and capacitor C_2. When the external pulse signal *post* arrives, the control switch φ_4 is turned on, and the capacitor C_2 is charged to VDD. With the end of the external pulse signal *post*, the capacitor C_2 passes through the NMOS transistor M_2 discharge, the voltage across the capacitor C_2 decays exponentially. The control switch φ_5 is used to transmit the voltage at both ends of the capacitor C_2 attenuated to the arrival of the external pulse signal *pre* to the NMOS transistor M_8; NMOS transistor M_8, NMOS transistor M_9 and NMOS transistor M_{10} constitute the weight update circuit is used to convert the voltage signal transmitted through the control switch φ_5 into a current signal, and transmit it to the capacitor C_3 through the control switch φ_6 to discharge the capacitor C_3, so as to realize the decrease of the synaptic weight when the postsynaptic pulse signal *post* arrives at the synaptic circuit before the presynaptic pulse signal *pre*. The NMOS transistor M_4 is controlled by the opposite signal of the external pulse signal *pre*. When there is no external pulse signal *pre* input, the NMOS transistor M_4 pulls down the gate voltage of the NMOS transistor M_8 to GND to avoid static power dissipation in the circuit when there is no signal control.

The NMOS transistor M_1 and NMOS transistor M_2 of the signal attenuation circuit in the synapse circuit work in the sub-threshold region. The NMOS transistor M_1 and NMOS transistor M_2 are used as leakage resistors, and the signal attenuation time constant can be controlled by adjusting the external bias voltage V_{leak}; The PMOS transistor M_7 and the NMOS transistor M_{10} in the weight update circuit also work in the sub-threshold region. The capacitor C_3 is used to store electric charges, and the change of the voltage across its two ends indicates the change of the synaptic weight.

4. Simulation Results

The transient simulation results of the synaptic circuit are shown in Fig. 3, Fig. 4, and Fig. 5.

Fig. 3 is a transient simulation diagram of the synaptic weight voltage when the time difference between the pulses emitted by the postsynaptic and presynaptic neurons of the synaptic circuit based on the STDP learning rule is a positive value. In Fig. 3, the first window represents the pulse sequence emitted by the pre-neuron, the second window represents the pulse sequence emitted by the post-synaptic neuron, the third window represents the change curve of the synaptic weight voltage, and the abscissa is the time. The simulation results show that the pulses fired by postsynaptic neurons arrive at the synapse later than those fired by presynaptic neurons, and the synaptic weight increases with the arrival of each pair of pulses.

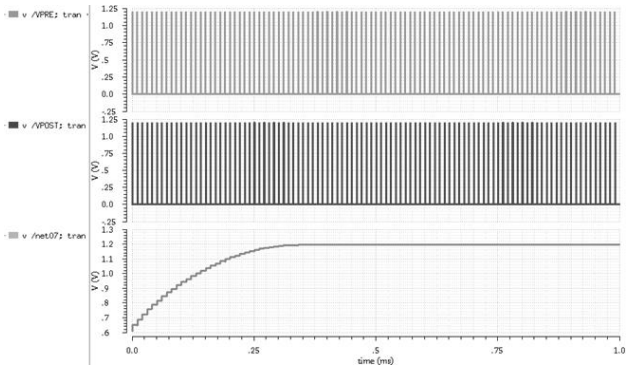

Fig. 3 Transient simulation of synaptic circuits with $td=t_{post}-t_{pre}>0$

Fig. 4 is a transient simulation diagram of the synaptic weight voltage when the time difference between the pulses emitted by the post-synaptic and pre-synaptic neurons is negative in the synaptic circuit based on the STDP learning rule. All windows in Fig. 4 have the same meaning

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as in Fig. 3 The simulation results show that the pulses fired by postsynaptic neurons arrive at the synapse earlier than those fired by presynaptic neurons, and the synaptic weight decreases with the arrival of each pair of pulses.

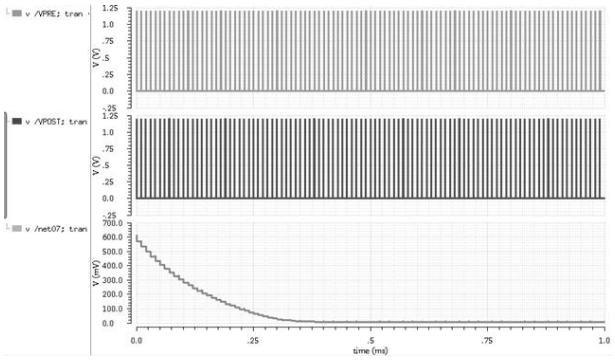

Fig. 4 Transient simulation of synaptic circuits with $td=t_{post}-t_{pre}<0$

Fig. 5 is a time window simulation diagram of the change of the synaptic weight voltage of the synaptic circuit based on the STDP learning rule, wherein the abscissa represents the time difference between the postsynaptic neuron and the presynaptic neuron firing pulses, and the ordinate represents the change value of the synapse weight voltage. The simulation results show that when the time difference between the postsynaptic neuron and the presynaptic neuron firing pulses is positive, the value of the synaptic weight increases exponentially with the increase of the time difference, and when the time difference between the time difference is negative, the value of the synaptic weight reduction decays exponentially with increasing time difference.

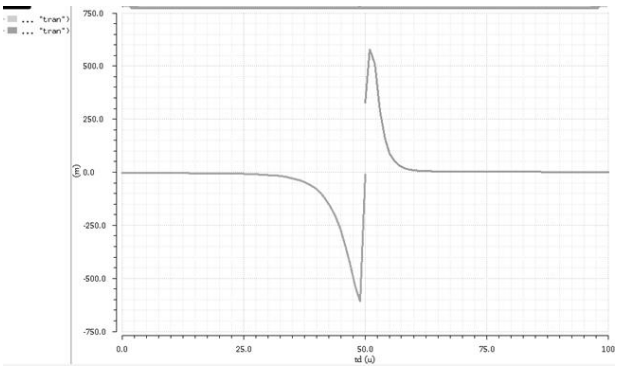

Fig. 5 Simulation result of synaptic weight learning window

5. Conclusion

In this paper, a synaptic circuit based on STDP learning rules is designed. The signal attenuation circuit in the synaptic circuit adopts the RC circuit to provide an adjustable time window for realizing the STDP learning rule, and cooperates with the control switch to transmit the changed voltage value to the weight update circuit. The control switch is controlled by the spiking signals fired by the presynaptic and postsynaptic neurons and is used to capture the time difference between the spiking signals fired by the presynaptic and postsynaptic neurons. The weight update circuit uses a voltage divider structure to convert the voltage into current to charge and discharge the capacitor C_3. Capacitor C_3 realizes charge change and charge storage. In addition, the circuit also adds an NMOS transistor before the weight update circuit to reduce power consumption and realize a low-power synapse circuit.

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