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Design for Testability of DMB Baseband SoC Chip

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Abstract

In order to ensure that the functions and performance of the chip after tape-out meet the design requirements, the testability design of the chip needs to be carried out. This paper introduces the testability design of the DMB baseband SoC chip based on the 0.11um process, and analyzes the uncontrollable factors in the DFT design and proposes solutions. The final test coverage rate is 98.20%, which meets the testability design. design requirements.

Keywords

SoC; DFT; Fault Coverage; Scan Chain.

1. Introduction

DFT is a design requirement that should be considered in the early stage of chip design, especially for SoC design[1], DFT runs through the front, middle and back ends of the design. The process of testing is mainly to control and observe the signals in the circuit to ensure the normal operation of the circuit. DFT technology is trying to increase the controllability and observability of the signal in the circuit to achieve the purpose of fault detection. It is a structural test based on the fault model. Controllability mainly refers to the use of external excitation to obtain defect characteristics, and the characteristic of transmitting such defect characteristics to the output port and performing it is called observability. There are three most commonly used design methods for testability at this stage: built-in self-testing, boundary scan, and scan path testing[2].

Scan path test, also known as scan design, is the most widely used testability design method in the industry. It is also the testability design scheme used in this article. It belongs to structural fault test and is often used in SoC design to solve sequential circuit testing[3]. the best solution. The main principle of scan design is to use testable scan flip-flops to replace the standard flip-flops inside the chip, so that all scan flip-flops are connected to form a scan chain in scan mode. Serial output response, so as to judge whether there is a fault in the design, and realize the control and observation of the internal test node.

The test target of the scan design is mainly the standard cells inside the chip[4]. The internal scan flip-flops are connected to form a scan chain for serial shifting to realize the input and output of the test data. The structure of the scan chain is shown in Figure 1, where Scan_en, Scan_in, Scan_out is an important part of the scan chain, Scan_en is used to control the switching of the scan chain circuit shift and capture, Test_mode is the test mode control port, used to control whether the chip enters the test mode, when Test_mode is equal to 1, it enters the scan test mode, and Test_mode will the clock of the control chip is switched to the scan clock, the reset signal is controlled to make it invalid, and the Scan_en signal is also equal to 1.

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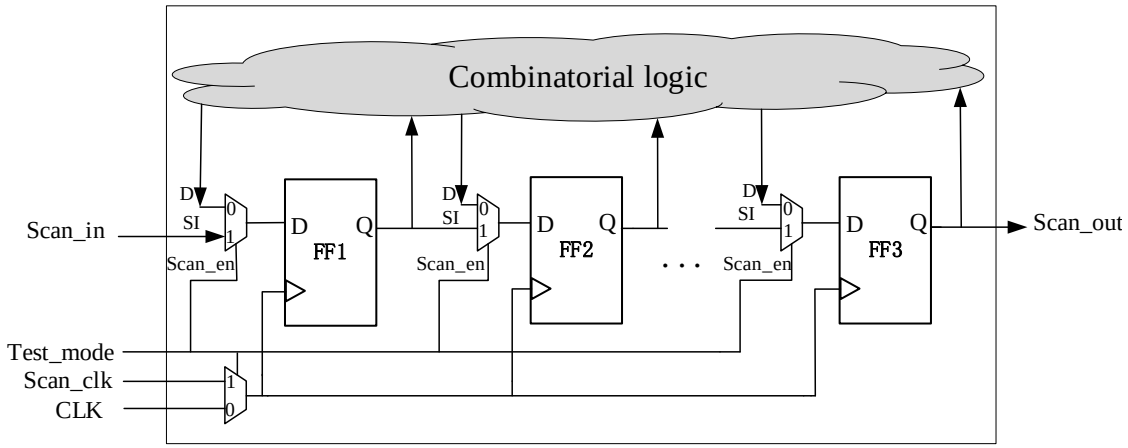

Figure 1. Schematic diagram of the scan chain structure

The steps of the scan test are generally to input the preset test data into the scan input port to form a test vector, and when the scan enable is 1, the test vector is serially shifted to the input port of each scan flip-flop, and then the scan is performed. The enable signal is released to 0, and the chip changes from the scan test mode to the normal working mode. After the combinational logic unit, the output value in this case is captured and sent to the output port through the scan chain under the control of the scan clock to compare with the expected value, to determine whether there is a fault inside the chip.

The standard for evaluating test quality is fault coverage, which is defined as the ratio of the detected faults to the percentage of faults that ATPG can test. Its expression is as follows

$$\text{Test Coverage} = \frac{\text{DT} + (\text{PT} \times \text{pt\_credit})}{\text{total faults} - (\text{UD} + \text{AU} \times \text{au\_credit})} \quad (1)$$

In the formula, DT represents the detected fault, PT represents the possible detected fault, UD represents the impossible to detect fault, AU represents the untestable fault, pt_credit defaults to 50%, au_credit defaults to 0%[5].

2. Design for controllability and observability

2.1. Controllability of gated clocks

The gated clock circuit is the most common method in chip low-power design. The design of gated clock can significantly reduce the dynamic power consumption of the chip by controlling the inversion of the clock signal. However, the introduction of the gated clock also brings a series of troubles to the test of the chip, and the uncontrollability of the gated clock will reduce the test coverage. The schematic diagram of the gated clock circuit is shown in Figure 2. The yellow shaded part represents measurable, and the gray shade represents unmeasurable. The enable logic in front of the gated clock cannot be passed on and has no observability. At the same time, the register unit of the gated clock is also not controllable, and the flip-flops behind the gated clock are not controlled by the scan clock during testing. Fault coverage is low.

The controllability design of the gated clock is mainly by adding an injection logic, adding an OR gate before the gated clock, and the gated enable signal EN and the scan enable signal Scan_en are connected to the gated clock after an OR gate. on the register unit. The controllability design of the gated clock is shown in Figure 3. Scan_en is used as a control signal. In test mode, Scan_en = 1, and the test vector is serialized into the scan chain; in normal function mode, Scan_en = 0, the value of control logic output EN It can be captured by the latch through the OR gate, and the EN signal can be observed. And the flip-flop controlled by the gated clock can be directly controlled by the input port CLK in the test mode, so the whole circuit is testable.

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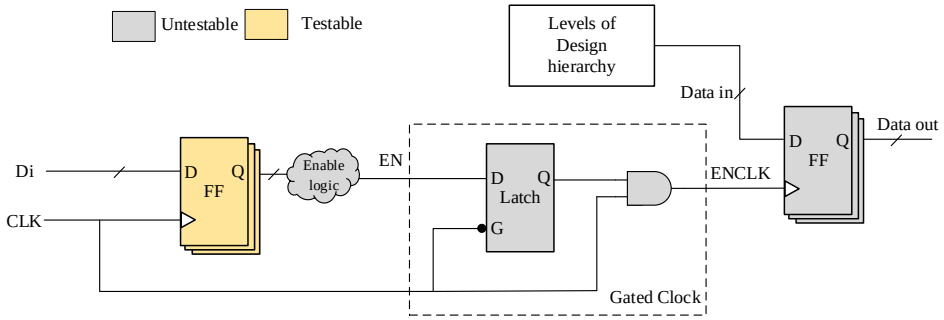


Figure 2. Circuit diagram of gated clock

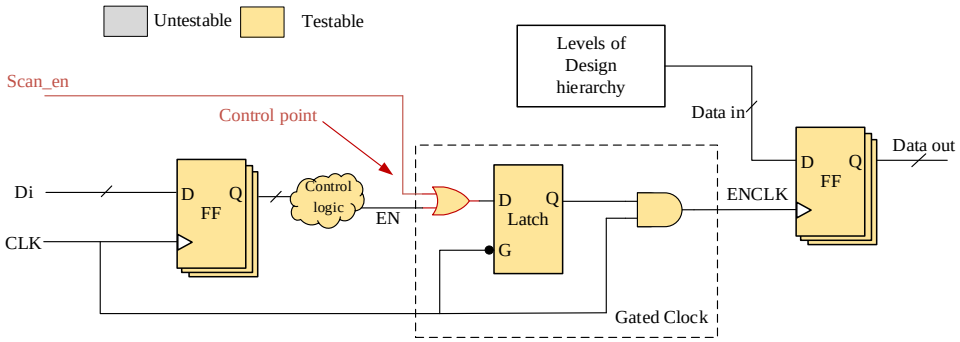
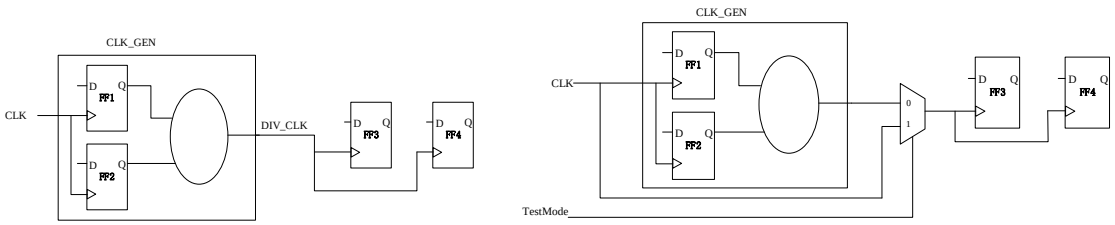


Figure 3. Controllability design of gated clock

2.2. Controllability of the clock generator

The clock generator circuit is also called frequency division circuit, which is relatively common in circuit design, especially in SoC design, where there are multiple clock domains, and the frequency division operation of the clock is inevitably performed inside the chip, resulting in many asynchronous clock circuits. In the DFT design, some flip-flops are not controlled by the test clock. As shown in Figure 4(a), the pulse signal of the test clock CLK cannot reach the flip-flops FF3 and FF4, which does not meet the clock controllability requirements in the test mode. These flip-flops cannot be included in the scan path, resulting in reduced scan coverage. In this case, a bypass circuit can be added, that is, adding MUX logic. During the test (TestMode = 1), the flip-flops FF3 and FF4 are directly controlled by the input port CLK. The controllability processing of the clock generator is shown in Fig. 4(b).



(a) clock generator circuit (b) Clock generator bypass processing

Figure 4. Controllability design of clock generator

2.3. Controllability of Asynchronous Reset

In the test mode, the reset pins of all flip-flop units are required to remain inactive when shifting, so as to ensure the reliability of scanning. The schematic diagram of the common asynchronous reset circuit in the chip is shown in Figure 5. In the test mode, the reset pins of flip-flops FF3 and FF4 are not controlled by the chip reset port RST, so they cannot be placed in the scan chain.

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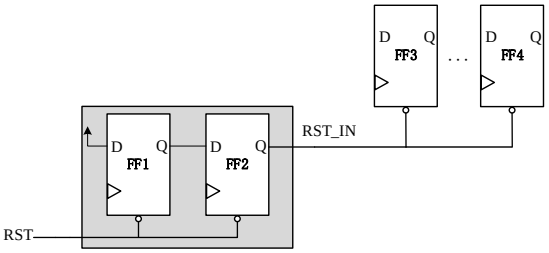
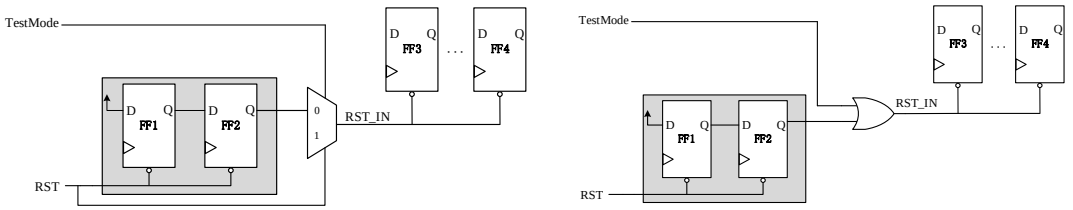


Figure 5. Schematic diagram of asynchronous reset circuit

The controllability design of the asynchronous reset port is shown in Figure 6. There are two processing methods, namely the bypass MUX processing in Figure 6(a) and the insertion logic processing in Figure 6(b), which can ensure that in the test mode (TestMode = 1), flip-flops FF3 and FF4 reset pins are controllable. The test coverage obtained with bypass MUX processing is usually higher than with inserted logic.



(a) Bypass MUX handling for asynchronous resets

(b) Insertion Logic for Asynchronous Reset

Figure 6. Controllability design of asynchronous reset circuit

2.4. Controllability of Memory

In the SoC chip, the amount of memory is generally relatively large. In the test mode, the memory does not work, and the circuit cannot be controlled and observed through them. For memory, Foundry will provide corresponding MBIST test methods. During the scan test, it is necessary to perform black box processing on the memory, and introduce a MUX structure to bypass all the memory, so that the signal can bypass the uncontrollable output port in the test mode, so that the surrounding circuits can be controlled and controlled. Observe, improve test coverage. The controllability processing of Memory is shown in Figure 7.

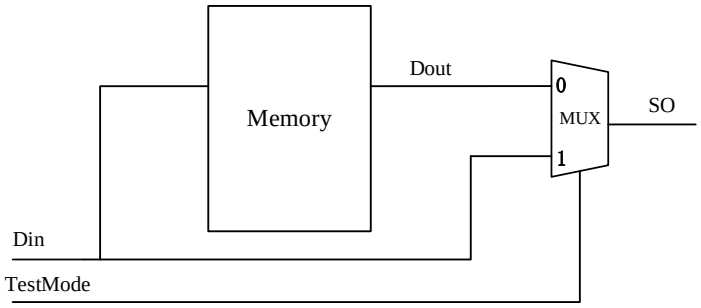


Figure 7. Controllability processing of Memory

3. Analysis of DFT results

In this paper, the baseband SoC chip uses a total of 12 scan chains. The scan chain report is shown in Figure 8. Each scan chain contains about 692 register units. The length of the scan chain is relatively similar. The scan path is from the scan input port gpio[0]~gpio [11] to the scan output port gpio[12]~gpio[23], the scan enable port is scan_en, and the scan clock multiplexes the clock port clk_24M.

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Scan_path	Len	ScanDataIn	ScanDataOut	ScanEnable	MasterClock	SlaveClock
I chain0	692	gpio[0]	gpio[12]	scan_en	clk_24M	-
I chain1	693	gpio[1]	gpio[13]	scan_en	clk_24M	-
I chain2	693	gpio[2]	gpio[14]	scan_en	clk_24M	-
I chain3	693	gpio[3]	gpio[15]	scan_en	clk_24M	-
I chain4	693	gpio[4]	gpio[16]	scan_en	clk_24M	-
I chain5	693	gpio[5]	gpio[17]	scan_en	clk_24M	-
I chain6	692	gpio[6]	gpio[18]	scan_en	clk_24M	-
I chain7	692	gpio[7]	gpio[19]	scan_en	clk_24M	-
I chain8	692	gpio[8]	gpio[20]	scan_en	clk_24M	-
I chain9	692	gpio[9]	gpio[21]	scan_en	clk_24M	-
I chain10	692	gpio[10]	gpio[22]	scan_en	clk_24M	-
I chain11	692	gpio[11]	gpio[23]	scan_en	clk_24M	-

Figure 8. Scan chain report

The ultimate goal of design for testability is to achieve the controllability and observability of all sequential units. In the design stage, it is necessary to consider improving test coverage and reducing test costs. The test coverage requirement is generally not less than 95%. The initial test coverage designed in this paper is only 78.09%, as shown in Figure 9(a), which is far lower than the design requirements. After using the above clock and reset controllability design scheme, the test coverage reaches 97.44%, as shown in Fig. 9(b).

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	209977
Possibly detected	PT	22
Undetectable	UD	5877
ATPG untestable	AU	58601
Not detected	ND	319
total faults		274796
test coverage		78.09%

(a) Initial test coverage

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	270213
Possibly detected	PT	11
Undetectable	UD	244
ATPG untestable	AU	6694
Not detected	ND	412
total faults		277574
test coverage		97.44%

(b) Test coverage after correction

Figure 9. Test coverage before and after correction

There are two ways to correct the test coverage. One is to modify the RTL code and add a bypass circuit. For example, for the frequency dividing circuit, the following modifications can be made, assign CLK_FF = TestMode ? CLK : CLK_DIV. The netlist can also be automatically corrected using the Autofix program of the DFTC tool.

The Autofix program can specify the input port test_mode as the test mode port to control all clock signals and reset signals. If there is a test DRC violation in the design, bypass logic and test points can be automatically inserted to improve the test coverage of the design. Autofix plays a great role in modifying frequency division clock circuits, gated clock circuits, and asynchronous reset circuits. The test point report inserted by Autofix is shown in Figure 10.

```
************ Test Point Plan Report ************
Total number of test points  : 118
Number of Autofix test points: 118
Number of Wrapper test points: 0
Number of test modes         : 1
Number of test point enables : 0
Number of data sources       : 2
Number of data sinks         : 0
************************************************

Dft signals:
 TestMode: test_mode (hookup pin: PAD_TestMode/C, sense: non-inverted)
 TestData: clk_24M (hookup pin: PAD_CLK24M/C, sense: non-inverted)
 TestData: rst_n (hookup pin: PAD_RST/C, sense: non-inverted)
```

Figure 10. Autofix test point insertion report

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The unprocessed memory cells in the circuit will also affect the test coverage and need to be bypassed. The main method is to add MUX logic to the RTL code, and test_mode is used to control switching. In test mode, the input data of the memory passes through the MUX logic. Output directly to the memory to complete the bypass to the memory. Modify the code as follows

assign ram_dout = test_mode ? ram_din : ram_dout_pre ;

In the above code, ram_dout is the output data of the MUX, ram_dout_pre is the normal read data of the memory, and ram_din is the input data of the memory.

After controllability of all memory cells, the final test coverage is 98.2%, as shown in Figure 11.

Uncollapsed Stuck Fault Summary Report

fault class	code	#faults
Detected	DT	273382
Possibly detected	PT	5
Undetectable	UD	291
ATPG untestable	AU	4702
Not detected	ND	300
total faults		278680
test coverage		98.20%

Figure 11. Final Test Coverage Report

After using Autofix correction and memory bypass processing, the test coverage of the chip has been significantly improved, meeting the design requirements of test coverage. The specific comparison results are shown in Table 1.

Table 1 Comparison of test coverage before and after optimization

stage	number of test failures	test coverage
Before optimization	274796	78.09%
Autofix fixes	277574	97.44%
Memory Bypass	278680	98.20%

The result of the physical layout of the scan chain is shown in Figure 12.

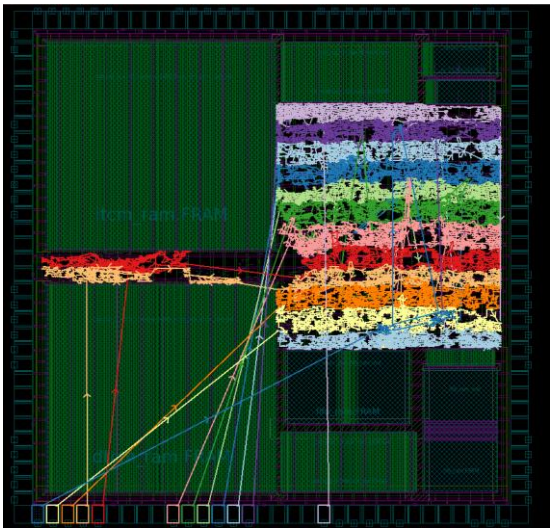

Figure 12. Physical structure of the scan chain

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4. Conclusion

This paper studies the testability design of DMB baseband SoC chip, analyzes and discusses the fault model and uncontrollable factors in the design, uses bypass processing and Autofix to improve the scan test coverage, and completes the testability design of the baseband SoC chip , a total of 12 scan chains are used, each scan chain contains about 692 register units, the scan port is directly multiplexed with the chip IO, and the final test coverage rate is 98.20%.

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