Design of Low-noise Transient Electromagnetic Receiver Based on FPGA

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Abstract

The transient electromagnetic signals are of much small amplitude in the late stage so they are easily submerged by electromagnetic noise. In this paper, a low-noise transient electromagnetic receiver is designed based on field programmable gate array (FPGA) to accurately and continuously record the late transient electromagnetic signals. In the system, parallel structure of amplifying circuit greatly reduce the voltage noise of the front solving the problem of differential amplifier that only the external noise can be mitigated. Besides, the data can be quickly and continuously sampled and stored by combing the FIFO buffer area in FPGA and Ping-pong buffer structure. The experimental results show that the level of the system noise is below 4μV and the performance of designed system is well stable. In all, the system can be applied in detecting the transient electromagnetic signals.

Keywords

FPGA, Low Voltage Noise, Parallel Amplifiers, Continuous Sampling, Ping-Pong Buffer.

1. Introduction

Time domain electromagnetic methods (TEM) are popular methods in fields of the geophysics, due to the advantages of large detection depth and high lateral resolution. The basic mechanism of the methods can be illustrated as follows. The transmitter emits a primary pulsed magnetic field into the ground by an ungrounded coil, which induces the excellent conductor under the ground to produce a secondary current (eddy current). Then the response of the secondary field with is measured by the receiving device in time domain. The received secondary field signal is a continuous curve with exponential attenuation. The signal decays very fast in the early stage. And it is of small amplitude in the late stage (usually in the order of microvolt), which is easily submerged by electromagnetic noise. Thus, it is important to accurately record the transient electromagnetic signals in the late stage.

The research on transient electromagnetic instruments started early and there are some mature products, such as the PROTEM system of Geonics in Canada, the V8 series of Phoenix in Canada, and the SIORTEM series of CSIRO in Australia. However, in China, the research on transient electromagnetic instruments begun at 1970, which is a little late. Recently, China University of Geosciences (Wuhan) has developed CUGTEM-4 transient electromagnetic instrument exploring resources under deep ground. And Jilin University has developed ATEM2 type transient electromagnetic instrument. In 2016, Su Fa developed a LabView-based transient electromagnetic receiving system. Yuan Guiyang has developed an ARM-based sampling device for induction current in 2017. Based on these research about the instruments, there are some key points. The front amplifiers in these instruments are always differential amplifiers, which can suppress the external common mode noises but can not effectively mitigate the noise form amplifiers. Besides, the main control units are always based on ARM or C-Rio. The controller from ARM is of lower power consumption but its internal resources are limited and the processing speed is slow somehow. Therefore, it can not continuously store the
data. The C-Rio controller is of high functional scalability and a short development cycle but its volume is large and the maximum power consumption is 38W, which is not suitable for outdoor experiments.

According to the analysis above, a low-noise transient electromagnetic receiver is designed in this paper based on FPGA, which is mainly composed of a pre-amplifier and a data acquiring and storing system. The equivalent input noises are reduced by paralleling the pre-amplifiers. Some theoretical analysis and simulations have been done to compare the noise level of single amplifiers and paralleled front amplifiers. The results shown that the parallel operation of amplifiers can achieve lower noise level. The data sampling system employs $\Sigma$-$\Delta$ modulation and over-sampling technology for analog to digital conversion. The storing system combines the internal buffer in FPGA with Ping-pong buffer structure to achieve quick and continuous storage. Finally, the effectiveness of the system is verified by experiments.

2. General Design of the System

The low-noise transient electromagnetic receiver in this paper consists of the front amplifier circuit, inversing amplifier circuit, data acquisition and storage module (A/D conversion circuit, FPGA and SD card), GPS synchronization module and power supply modules. The diagram of the general design of the system is shown in Fig.1. The synchronization of transmitter and receiver is realized by GPS. The secondary field signal received by the receiving coil is converted into voltage signal after sampling. The voltage signal is amplified by low-noise front amplifiers and inverted by inversing amplifiers to form a differential signal with the initial signal. Then the signal is converted into digital signal by A/D conversion circuit. The sampling system and storing system pick up the data and storing them in the SD card. All the sub-part in the system is powered by the power modules separately.

![Diagram of the general design of the system](image)

Figure 1: General design of the system

3. Design of the Pre-amplifiers

3.1. Noise Analysis and Low Noise Design

The noise level of the pre-amplifiers, the first stage of the circuit, limits the resolution of the receiver and directly determines the minimum amplitude of the measured secondary field signal. In practice, the noises inside and outside the circuit are inevitable, which will disturb the pre-amplifiers and affect the performance of the system. In outdoor experiments, power frequency noise, motion noise, geomagnetic noise and other external noises will be mixed into the secondary field signal at the beginning of measuring. It is difficult to remove these noises by analog circuits and their influences on secondary field signal are generally suppressed by effective shielding and digital filtering in the later. And the white noise can be suppressed by differential amplification.

The noises inside the circuit mainly include resistance noises, analog power noises and amplifier noises. The former two kinds of noises can be reduced by selecting proper
components, reasonable PCB layout, and filtering capacitors. The noises of amplifiers depend on the current noise density, $I_n \, (pA/\sqrt{Hz})$, and current noise density, $V_n \, (nV/\sqrt{Hz})$. When the overall impedance of the receiving coil is $Z_R (\Omega)$, the voltage noises of the coil inducing by the current noises can be expressed as

$$V_{in} = I_n \times Z_R$$

(1)

Always, there is $V_{ns} << V_n$. Thus, it is much important to mitigate the noise in the selection of amplifiers and design of circuit. In the parallel configuration of amplifiers, the n noise sources are added together. Then the noises of amplifiers increase by a factor of $\sqrt{n}$ while the amplitude of related input signals is n times larger after summation and amplification. Hence, the noises of amplifiers are lowered and the signal to noise ratio (SNR) is increased by parallel operation of amplifiers in this paper.

The ultra-low noise instrumentation amplifier, AD8429, from ADI has a two-stage three-op amplifier topology. The first stage acts as differential amplification and the second stage is a differential amplifier that eliminates common-mode voltage and provides additional amplification. The amplifier is easy to be designed, whose gain is set by a single resistor. Besides, the amplifiers are of very low input and output voltage noise, and a very high common-mode rejection ratio. The parallel pre-amplifier based on AD8429 has a differential amplifier structure and a parallel amplifier structure at the same time. The circuit is of simple structure, low power consumption, and low noise. It is well suitable for transient electromagnetic detection. Thus, the ultra-low noise instrumentation amplifier, AD8429, is selected.

3.2. Analysis and Calculation of the Circuit Noises

The amplifying circuit for a single amplifier, AD8429, is shown in Fig. 3, where $R_1$ and $R_2$ are the protection resistors of the input, and $R_c$ is the resistance adjusting the gain. The background noise at the input of the circuit is mainly caused by three factors: protection resistance noises, voltage noises of and current noises of the instrument amplifier.

Protection resistance noises $E_R$: There are always some noises in any resistors, which is proportional to the square root of the resistance value. The resistance noise at room temperature is

$$E_R = 4nV/\sqrt{Hz}\times\sqrt{R}$$

(2)

where $R$ is the resistance value, whose unit is kΩ.

(2) Current noises $E_I$: The noises are introduced by protecting resistors and can be calculated by multiplying the resistance value and current noises.
(3) Voltage noises $E_V$: The noises are concerned with input voltage noises $E_{\text{in}}$, output voltage noises $E_{\text{no}}$, and $R_G$, which can be specifically expressed as

$$E_V = \sqrt{(E_{\text{no}}/G)^2 + E_{\text{in}}^2 + E_{RG}^2}$$

where the gain is $G=1+6000/R_G$.

The background noise at the input end of the circuit is

$$E_{R\text{TI}} = \sqrt{E_{RT}^2 + E_{I}^2 + E_{V}^2}$$

In the practical circuit, the protection resistors, $R_1$ and $R_2$, are neglected at the positive and negative input ends while several regulator tubes are employed for over-voltage protection. Therefore the input background noise is numerically equal to the voltage noise. The $E_{R\text{TI}}$ can be calculated when the magnification times is 100 and the result is 1.5nV. The background noises from the output port can be $E_{R\text{TO}} = E_{R\text{TI}} \times G = 150.0nV$. The noises of a single amplifier are verified by simulation in LT-spice and the background voltage noise density from output port is presented in Fig.4. It can be seen that the voltage noise seen from the output is approximately equal to 149.4nV within the frequency range of 1kHz-100kHz, which is consistent with the calculated results.

![Figure 4: Voltage noise density of single amplifier circuit from the output port](image)

When two instrument amplifiers are paralleled, the voltage noises increase only twice. In practice, the noise of two amplifiers is averaged after summation. Thus, the output voltage noise is $E_{R\text{TO}} = \sqrt{2E_{R\text{TI}}/2} = 106.0nV$. Some simulation verifications are carried out and the background voltage noise density at the output end was obtained as shown in Fig. 5. It can be seen that, the voltage noise at the output end is approximately equal to 105.8nV within the frequency range of 1kHz-100kHz. The results are consistent with the theoretical results, which verifies that the parallel amplification circuit could mitigate the circuit noises.

![Figure 5: Voltage noise density of two paralleled amplifiers from the output port](image)
4. System of Data Sampling and Storing

4.1. Analog-to-Digital Conversion

The conversion precision of data acquiring system is closely related to the number of bits in the analog-to-digital conversion chip. In this paper, the 24-bit A/D converter, AD7764, from ADI is selected. The sampling rate is up to 312kHz, which meets the requirements of transient electromagnetic detection. The peripheral settings and internal structure of the chip are shown in Fig. 6.

Figure 6: Peripheral settings and internal structure of AD7764

The ADC is driven by differential signals. Since the output of the pre-amplifier is a unipolar signal $V_{in+}$, the output signal of the pre-amplifier should be reversed to obtain $V_{in-}$. Then a pair of differential signals will be produced to drive the AD7764. The 40M active crystal vibration is set in the periphery to provide a stable working clock for the internal modulator. A 4.096V voltage reference source is provided by the ADR444 to serve as a voltage reference for modulators and differential amplifiers. A differential amplifier is integrated into the ADC for conversion of electric level and signal buffering, which requires a front-end smoothing filter as shown in Fig. 7. The on-chip modulator adopts the $\Sigma$-$\Delta$ modulation technology. The data will be oversampled to make the quantized noise distributed in the 0-20MHz frequency band because its clock frequency is much higher than the data output frequency. Then the noise within the bandwidth of the transient electromagnetic signal can be suppressed. Finally, the data is sent to FPGA by SPI communication interface after digital low-pass filtering.

Figure 7: Configuration of on-chip differential amplifier

4.2. Continuous data storing

The data must be stored in time because the receiver continuously acquire data. The way of data transmission between the FPGA and the SD card is the block of data transmission. Each
A data block is stored into the SD card at high speed. And one SD2.0 writing order require 512 times writing operation, each time 1 byte. If the data received by FPGA are directly put into the SD card without the cache, some of the data will be discarded when the SD card is busy with writing operation. Therefore, it is necessary to temporarily store the data in the cache area before storing it in SD.

In this paper, the FIFO cache area is set up inside FPGA. However, the storage resources of FPGA are limited and the cache areas cannot meet the temporary storage requirement of plenty of data. Thus, the FIFO cache area is divided into two parts and the ping-pong cache structure is employed to achieve real-time storage of a large amount of data. The data transmission diagram is shown in Fig.8.

![Figure 8: Diagram of data transfer with ping-pong cache structure](image)

Figure 9: The attenuation curve at a measuring point in the Greater Hinggan Mountains

The ADC begin to acquire data under the controlling of FPGA. Then the data are conveyed to FPGA by SPI bus, which are stored in SD card after data cache. In the FPGA, the input data are allocated to two cache areas, FIFO1 and FIFO2, by the data selection unit. First, the data from AD are stored in FIFO1. When the FIFO1 is full, the data will be stored in FIFO2 by switching the input data selection unit. Then the data from FIFO1 is passed to the output data selection unit. When the FIFO2 is full, the data are stored in FIFO1 again. Then the data in FIFO2 is passed to the output data selection unit. The above operation is repeated. The ping-pong cache structure is regarded as a whole module. Viewing from the input and output of the module, the data is continuous. Therefore, the ping-pong cache structure can realize continuous real-time storage of data.
5. **Experimental results and Analysis**

Based the principle of the hardware circuit above-mentioned, the transient electromagnetic receiver is designed and tested in field measurement experiments for exploring the lead-zinc ore in Xinlin, Daxing anling, in September 2020. The emitted current waveform is bipolar trapezoid wave with amplitude of 18A. The turn-off time is 300μs and the frequency is 12.5Hz. The quadratic field attenuation curve of a certain measurement point is shown in Fig.9 when the amplification factor of the pre-amplifier circuit is 35. It be seen that the initial amplitude of the secondary field is 0.645mV and the late signal, namely the peak-to-peak value of the system noise, is less than 4μV, which meets the requirements of transient electromagnetic detection.

6. **Conclusion**

In this paper, a low-noise transient electromagnetic receiver is designed based on FPGA. The system employes FPGA as the main control unit. By parallel amplification, A/D acquisition and ping-pong cache, low-noise acquisition and high-speed continuous storage for transient electromagnetic secondary field signals can be achieved. The system has the advantages of low noise, high sensitivity and simple circuit structure. The verifications of the system are conducted by simulation and field experiments. The results show that it can be applied in the transient electromagnetic detection.

**References**


